


Enrico Caruso 14
Muxless Schematics Document
Ivy Bridge & Sandy Bridge
Intel PCH
2012-01-03
REV : X02

DY : None Installed
PSL: 10mW internal schematic
UMA: UMA ONLY installed
OPS: Optimus solution installed.
Surge: For GO Rural config stuff.
GIGA: For GIGA LAN config stuff.
LPC : Reserve for LPC debug card
POP : Reserve for solve "POP" sound issue

<Variant Name>		
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Cover Page		
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Block Diagram (Discrete)

Project code:

Inspiron:91.4TY01.001

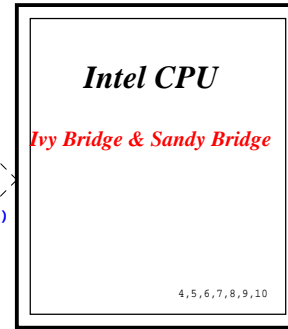
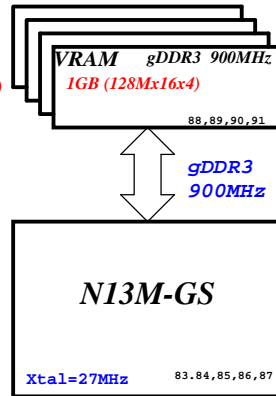
Vostro :91.4UA01.001

PCB P/N :48.4TY02.0SC

Revision:11282-SC

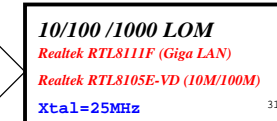
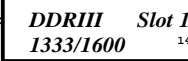
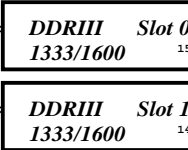
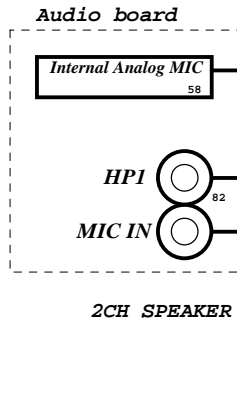
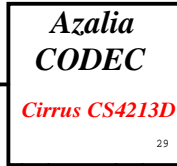
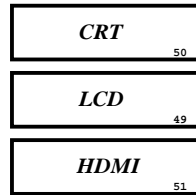
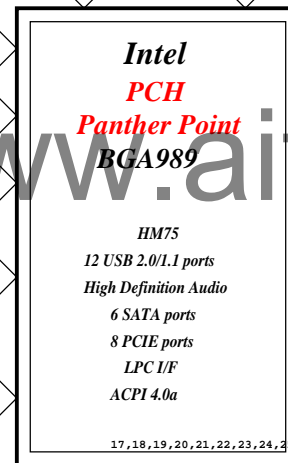
##OnMainBoard

Hynix:72.52G63.A0U (HT31P\$AA)
Samsung:72.42164.D0U (JP0F2\$AA)



FDIx4x2

DMIx4



USB 2.0 x 1

USB 2.0 x 1

USB 2.0 x 1

USB 2.0 x 2

DDRIII 1333/1600 Channel A

DDRIII 1333/1600 Channel B

PCIE x 1

PCIE x 1

PCIE

100MHz

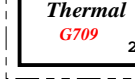
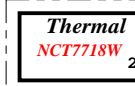
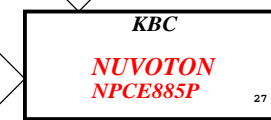
2.5Gbps

USB 2.0

480Mbps

LPC Bus

33MHz



SYSTEM DC/DC		48
APL5916		
INPUTS	OUTPUTS	
DCBATOUT	0D85V_S0	

CPU DC/DC		42~44
VT1318+1323		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	

SYSTEM DC/DC		45
TPS51219		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VTT	

SYSTEM DC/DC		41
TPS51125		
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5	

SYSTEM DC/DC		46
TPS51216R		
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	

GFX DC/DC		44
VT1318+1323		
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFXCORE	

VGA		92
ADP3211		
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	

TI CHARGER		40
BQ24707		
INPUTS	OUTPUTS	
+DC_IN_S5 +PBATT	DCBATOUT	

SYSTEM DC/DC		47
RT8068A		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S0	

Switches		93
INPUTS	OUTPUTS	
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0	

PCB LAYER		
L1:Top L2:GND L3:Signal	L4:Signal L5:VCC L6:Bottom	

<Variant Name>

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Title **Block Diagram**

Size A3 Document Number **Enrico Caruso 14 MLK DIS** Rev **X02**

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Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation! DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms \pm 5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms \pm 5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms \pm 5% pull-up resistor to PCH_VccDFTERM.
SATA1GP/ GPIO19	Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Panther Point require SPI flash connected directly to the Panther Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel® HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug. This signal has a 20k internal pull down resistor.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform. Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vinmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.
GPI015	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
GPI028	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-k to 10-k pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7k resistor to ensure proper strap setting when use as the chipset test interface. Refer to the latest platform debug design guide and platform design guide for more details. NOTE: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPI029/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft strap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort 0: Enabled - An external Display Port device is connected to the Embedded Display Port pull-down to GND through a 1K \pm 5% resistor to enable port	1
CFG[6:5]	PCIe Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

Sandy Bridge + Ivy Bridge Compatibility Requirements

Pin Name	Configuration	Schematic Notes
DDR3 VREF	Sandy Bridge + Ivy Bridge Ivy Bridge	DDR3 VREF M1 and M3 Guidelines are required. Note: The M3 traces are routed to the Sandy Bridge Processor reserved pins. No change.
PROC_SELECT# DF_TVS	Sandy Bridge + Ivy Bridge Ivy Bridge	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K \pm 5% series resistor. PROC_SELECT# also needs a 2.2K \pm 5% pull up resistor to PCH_VccDFTERM rail. No change.
VCCIO VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a requirement for a separate VCCIO VR for Sandy Bridge + Ivy Bridge compatibility. No change.
VCCSA_SEL	Sandy Bridge + Ivy Bridge Ivy Bridge	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller. No change.
Layout Requirement on PCI Express Gen3	Sandy Bridge + Ivy Bridge Ivy Bridge	The total motherboard length for a pair of consecutive PCI Express Tx lanes be length matched within 100 mils (2.54 mm) No change.
GT Core VR Implementation	Sandy Bridge + Ivy Bridge Ivy Bridge	Depending on the PDBG specifications, some IVB GT2 SKUs may require a new VR controller and 2 phase VCC GT core VR. No change.
Processor PCI Express Graphics Guidelines	Sandy Bridge + Ivy Bridge (PCIe Gen3) Ivy Bridge	To support Gen 3 PCI Express Graphic, the value of the AC coupling capacitor should be 180 - 265 nF. No change.

Power Plane

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
SV_S0 ID3V_S0 ID4V_S0 ID5V_S0 ID6V_VTT ID8V_S0 ID7V_S0 VCC_CORE VCC_DPFCORE ID4V_VGA_S0 ID3V_VGA_S0 ID_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	ACTIVE IN S0	CPU Core Rail Graphics Core Rail
SV_DIEBK_S3 ID3V_S3 ID3V_VREF_S3	5V 1.5V 0.75V	S3	
RT# D0A10OUT ID_S5 SV_AUX_S5 ID3V_S5 ID3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
ID3V_LAN_S5	3.3V	NOL_RH	Legacy WGL
ID3V_AUX_EBC	3.3V	D0W, Sx	ON for supporting Deep Sleep states
ID3V_AUX_S5	3.3V	G1, Sx	Powered by Li Coin Cell in G1 and +V3ALM in Sx

PCIe Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	Onboard LAN
LANE7	X
LANE8	X

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

<Variant Name>



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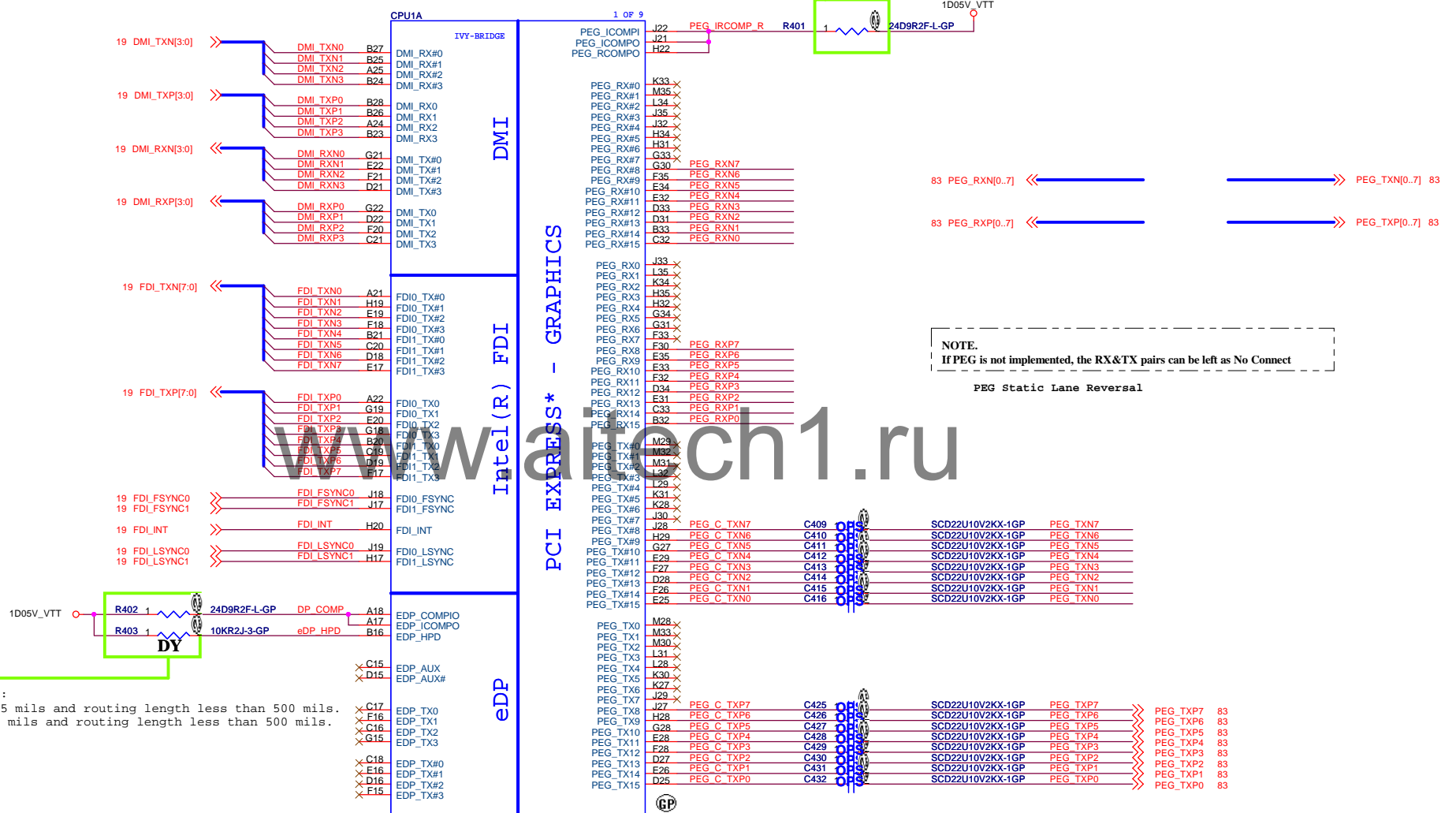
SSID = CPU

Layout Note:

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



62.10055.551

2nd = 22.10252.171

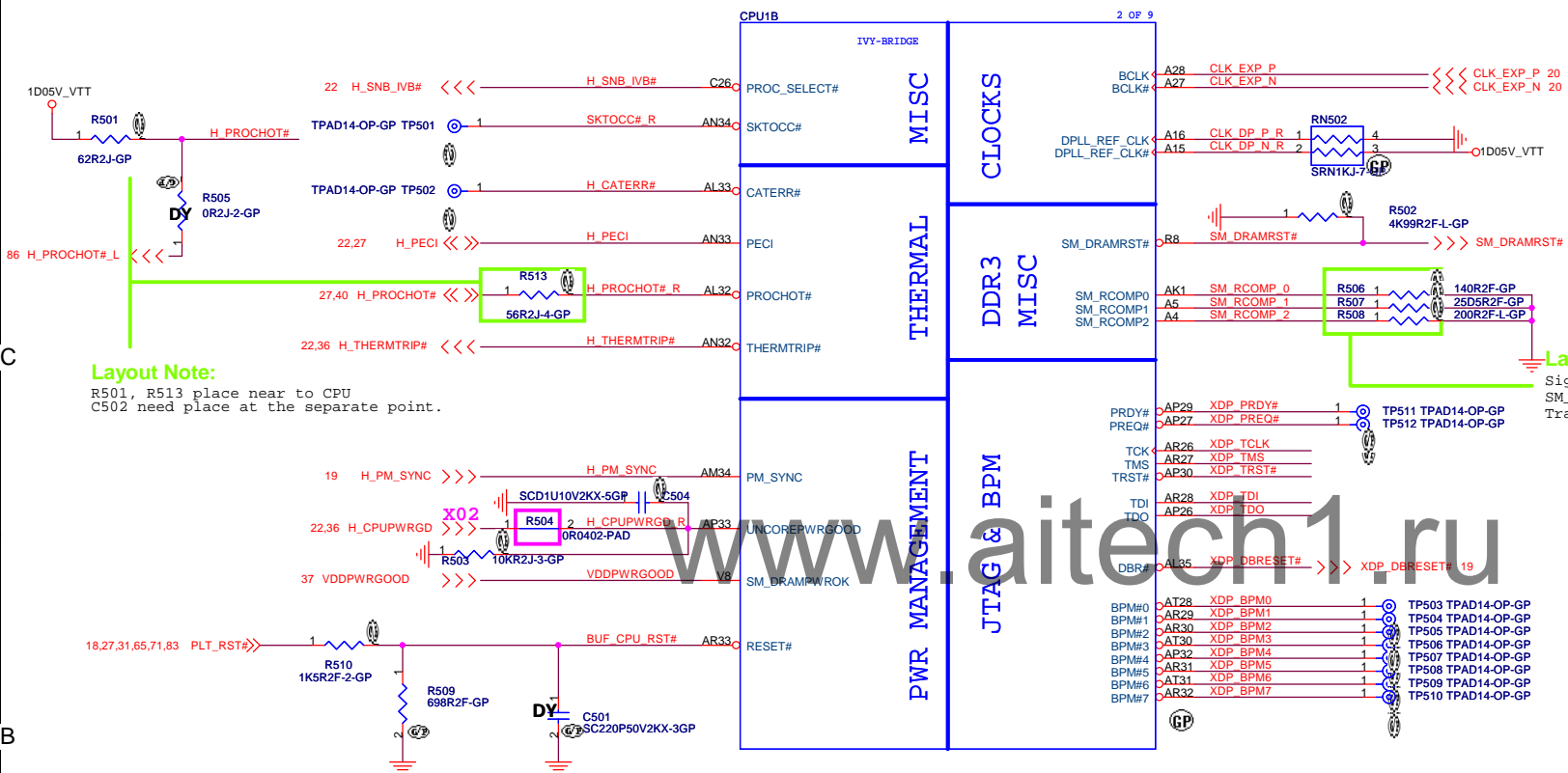
3rd = 62.10040.821

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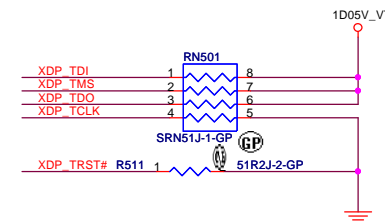
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CPU (PCIE/DMI/FDI)
Size A3 Document Number
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SSID = CPU



Layout Note:
R501, R513 place near to CPU
C502 need place at the separate point.

Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil



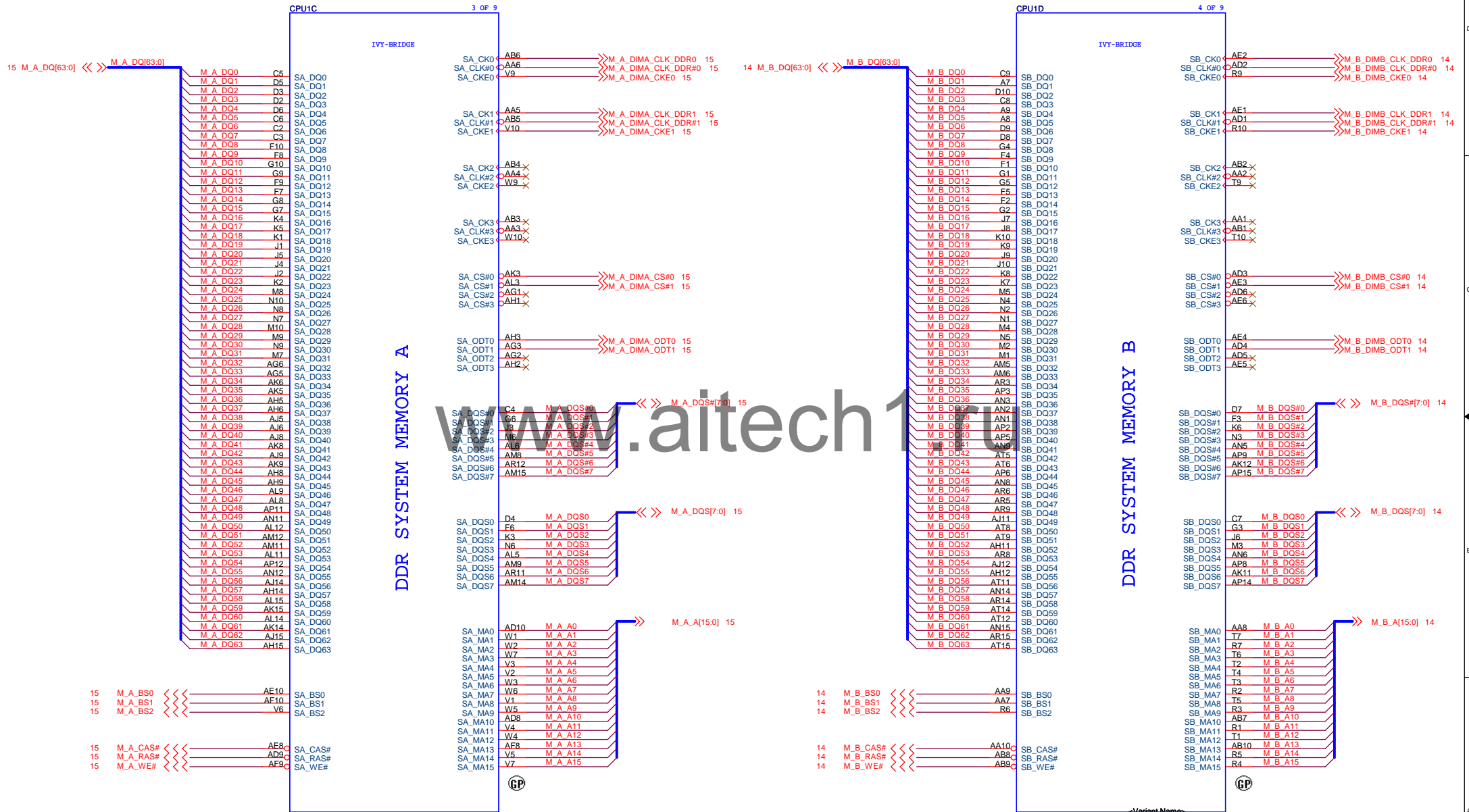
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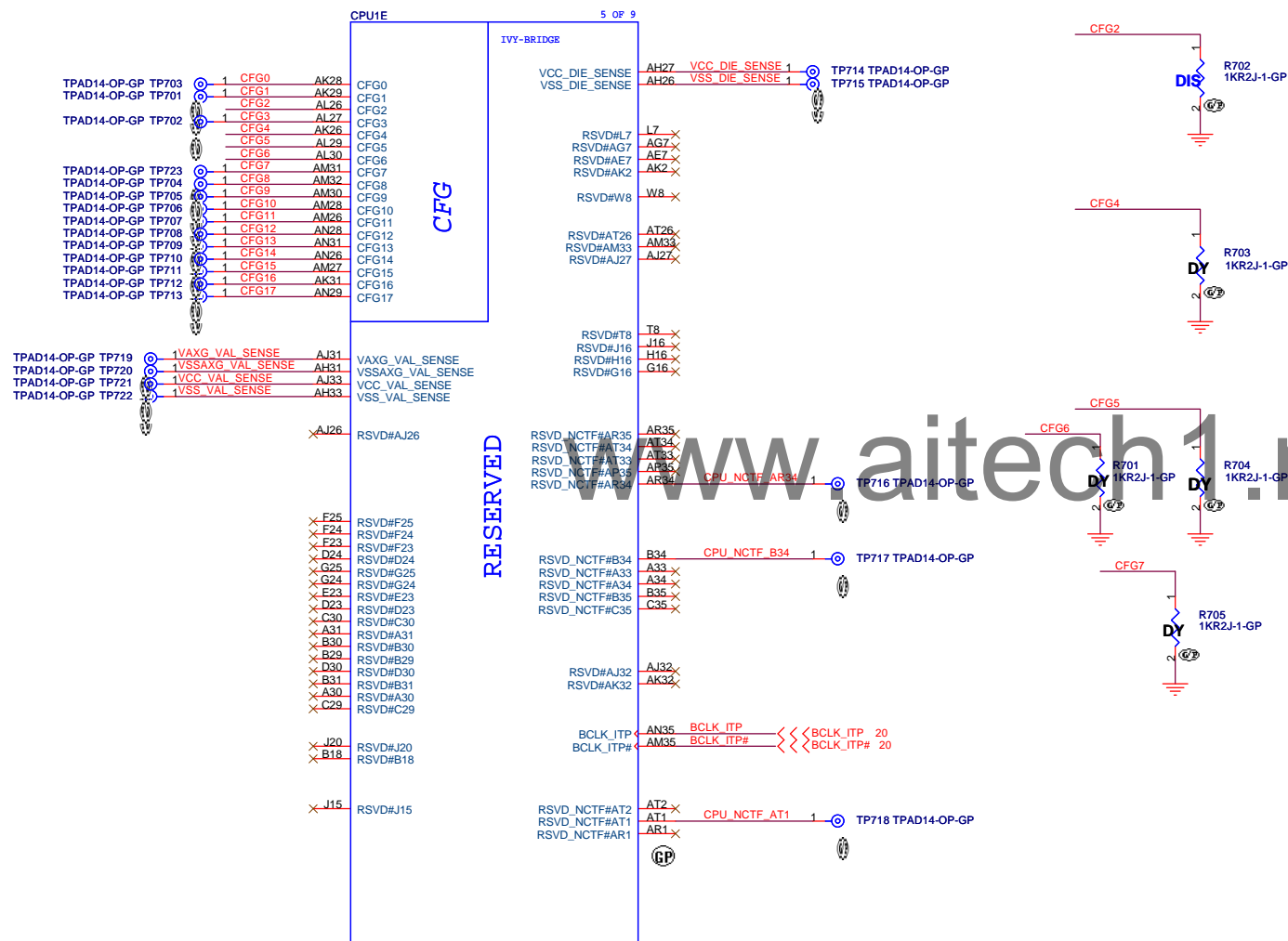
Title **CPU (THERMAL/CLOCK/PM)**

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SSID = CPU



SSID = CPU



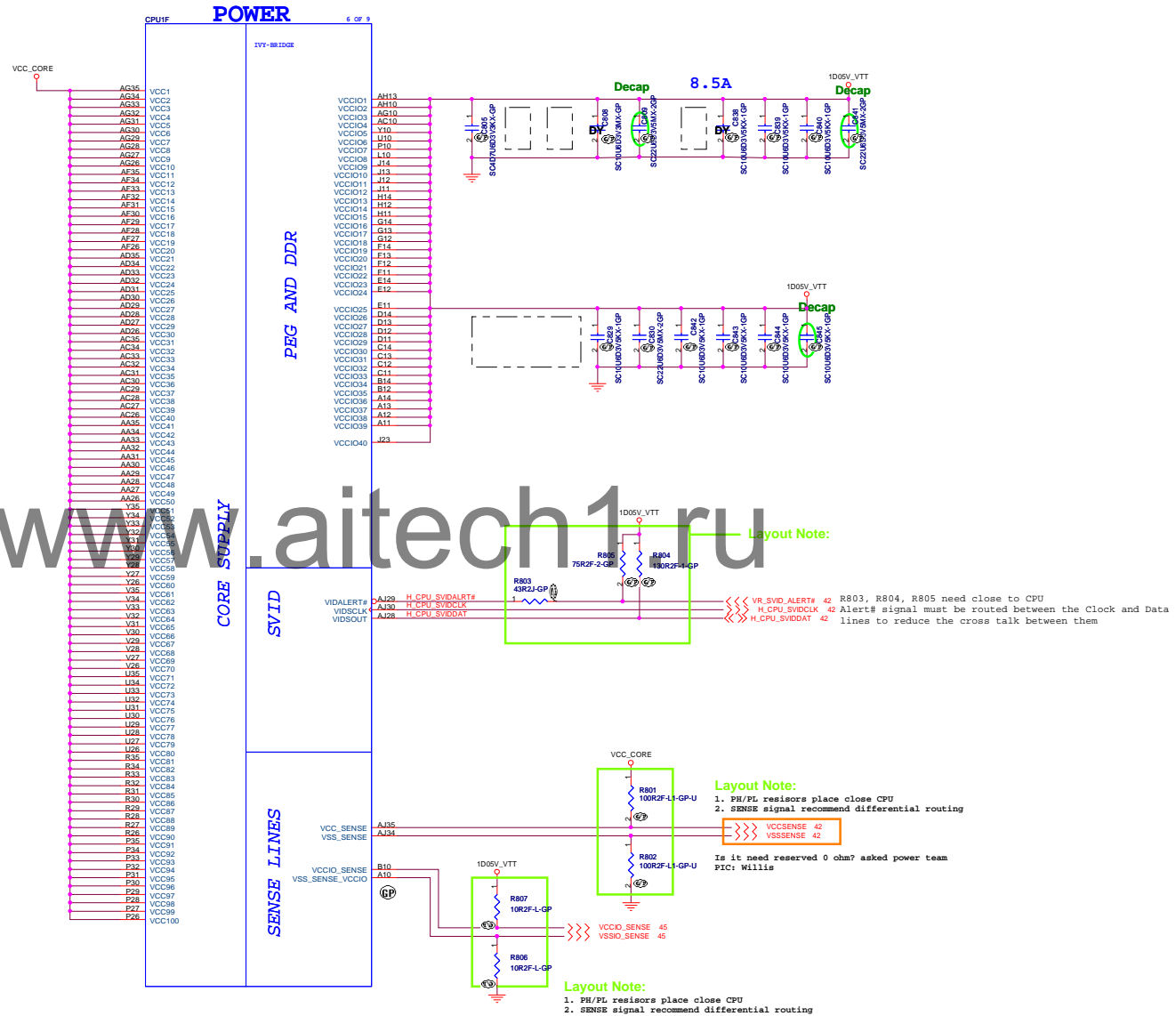
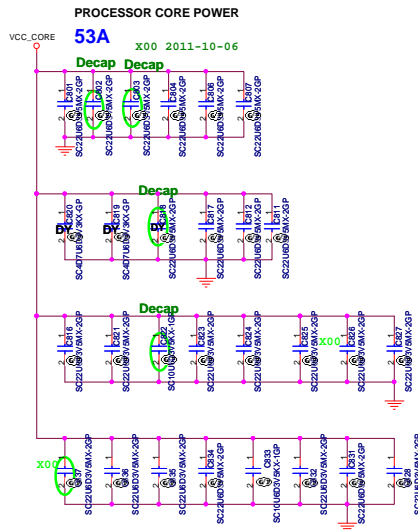
PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

Display Port Presence Strap	
CFG[4]	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(DC)	0.3-1.35	53
VAXIO(DC)	0-1.3	33
VCCIO	1	8.5
VDDQ	1.5	10
VCCSA	0.9	6
VCCPLL	1.8	1.5

Refer to PDDG rev 0.8



SSID = CPU

POWER

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE (DC)	0.3~1.35	53
VAXG (DC)	0~1.3	33
VCCIO	1	8.5
VDDQ	1.5	10
VCCSA	0.9	6
VCCPLL	1.8	1.5

Refer to PDDG rev 0.8

Layout Note:

1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Layout Note:

1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

79.33719.20L

2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:

- 1 x 330 uF
- 6 x 10 uF

Do not have 1 x 330 uF

VCCSA Output Decoupling Recommendation:

- 1 x 330 uF, 6m
- 2 x 10 uF at Bottom Socket Cavity
- 1 x 10 uF at Bottom Socket Edge

Do not have 1 x 330 uF

R910 close to pin H23.

VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
IV & ULV 0.85	0	1
Others 0.8	1	0
0.725	1	0
0.675	1	1

<Variant Name>

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Title CPU (VCC GFXCORE)

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GRAPHICS

SA RAIL DDR3 - 1.5V RAILS

1.8V RAIL

MISC

VCCIO_SEL:
SNB: Floating
IVY: GND

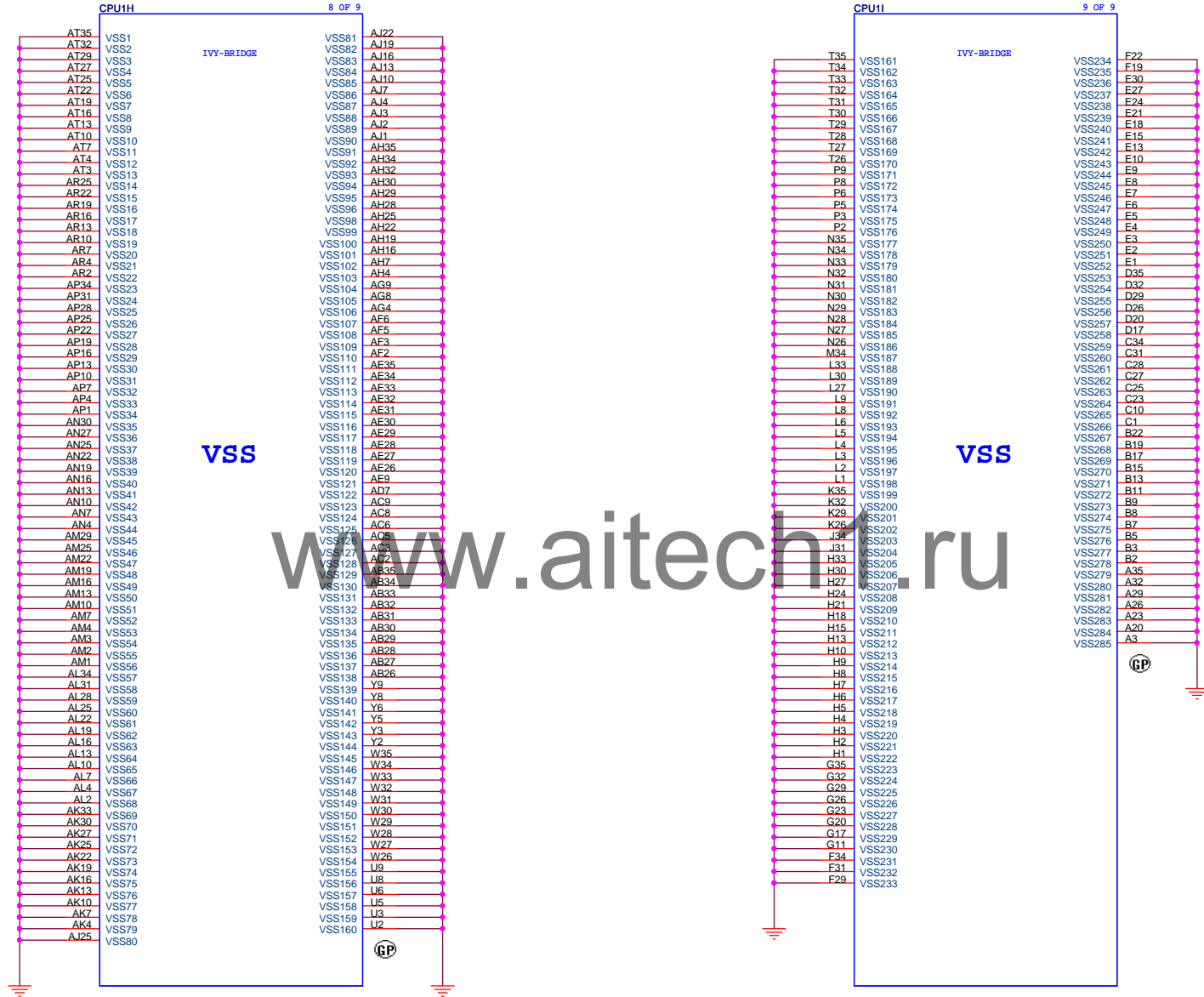
VAXG Output Decoupling Recommendation:

- 2 x 470 uF at Bottom Socket Edge
- 2 x 22 uF at Top Socket Cavity
- 4 x 22 uF at Top Socket Edge
- 2 x 22 uF at Bottom Socket Cavity
- 4 x 22 uF at Bottom Socket Edge

Do not have 2 x 470 uF

1.5A
1.8V_S0
SC10U02KX-1GP
C987
C988
C989
C990
C991
C992
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C994
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SSID = CPU



(Blanking)

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<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

BDP

Size
A3

Document Number
Enrico Caruso 14 MLK DIS

Date: Friday, December 30, 2011

Rev
X02

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(Blanking)

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<Variant Name>



Wistron Corporation
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Title

Size
A3

Document Number
Enrico Caruso 14 MLK DIS

Date: Friday, December 30, 2011

Reserved

Rev
X02

Sheet 12 of 104

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<Variant Name>



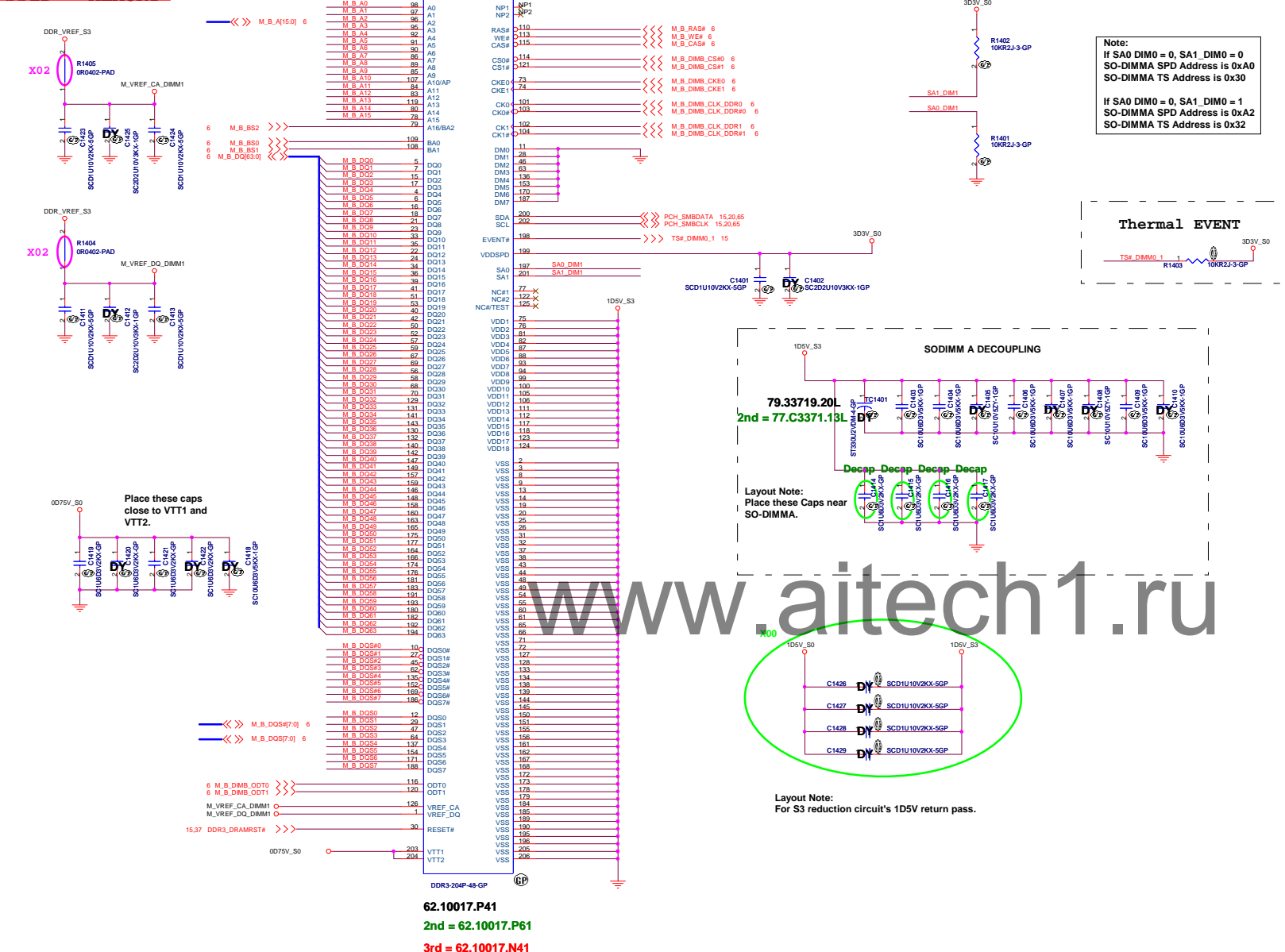
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

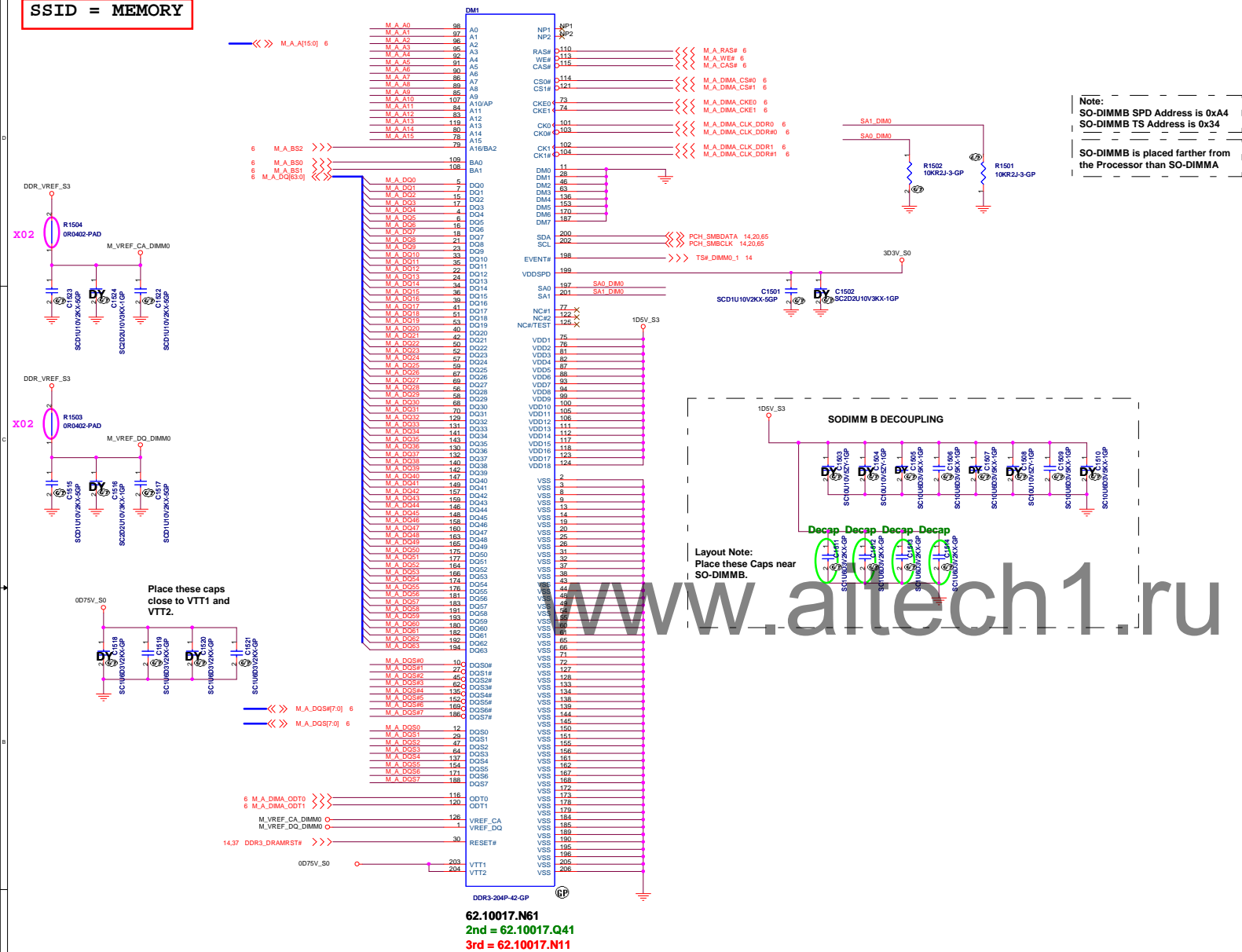
Reserved

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 13 of	104

~~SSTD = MEMORY~~

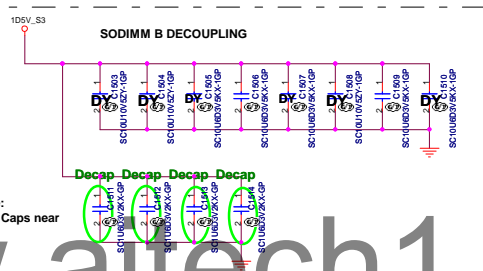


SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near
SO-DIMMB.

Place these Caps near SO-DIMM.

(Blanking)

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<Variant Name>



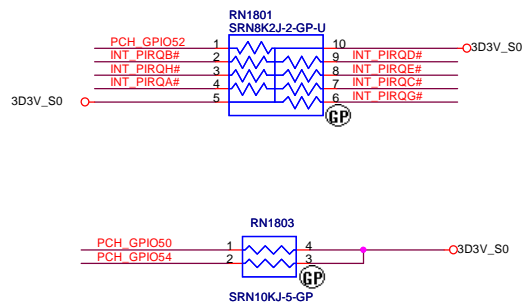
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

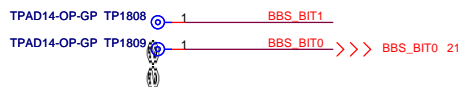
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 16 of	104

SSID = PCH



USB3.0/2.0 Mapping Table

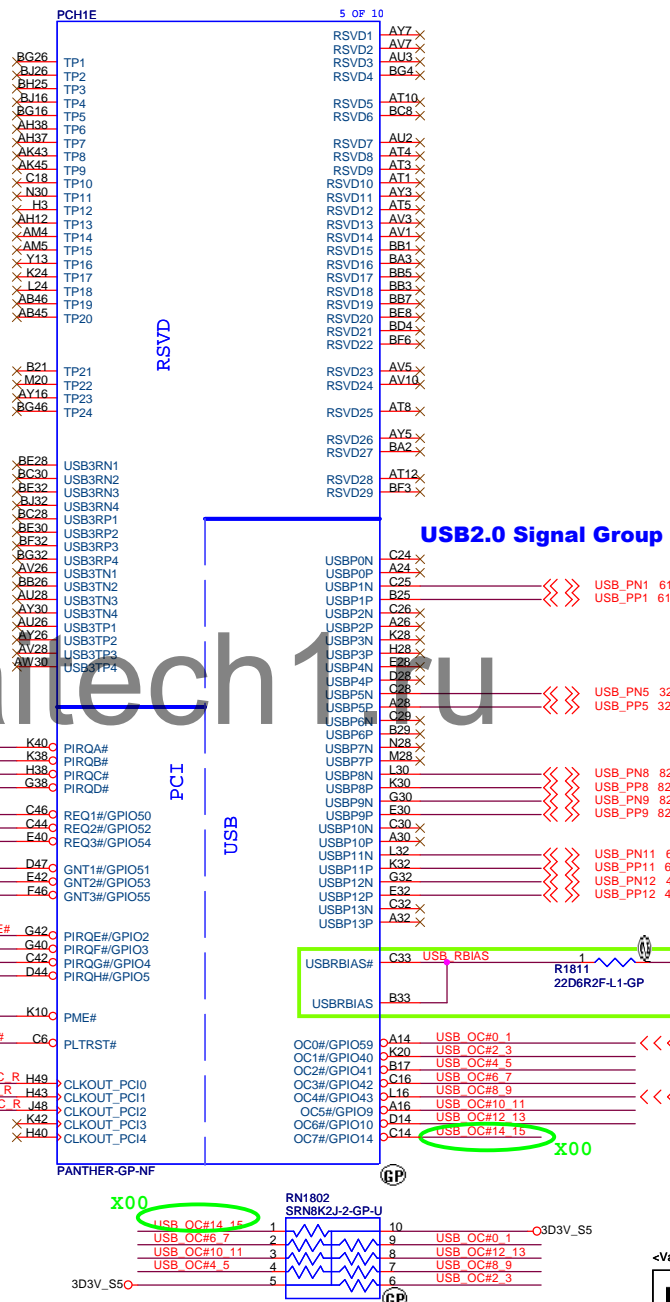
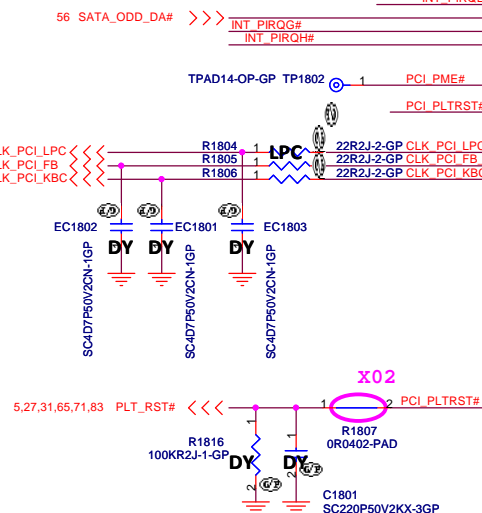
USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3



Boot Bios Strap		
GNT1#/GPIO51	SATA1GF/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



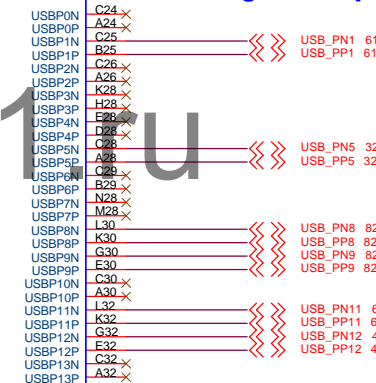
A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



USB Table

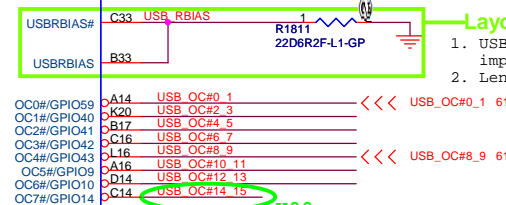
Pair	Device
0	NC
1	USB2.0 port1
2	NC
3	NC
4	NC
5	Card reader
6	NC
7	NC
8	USB2.0 port2
9	USB2.0 port3
10	NC
11	Mini Card1
12	CAMERA
13	NC

USB2.0 Signal Group



—Layout Note:

1. USBBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil



<Variant Names>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (PCI/USB/NVRAM)

Size

Document Number	
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Enrico Caruso 14 MLK DIS

Date: Tuesday, January 03, 2012

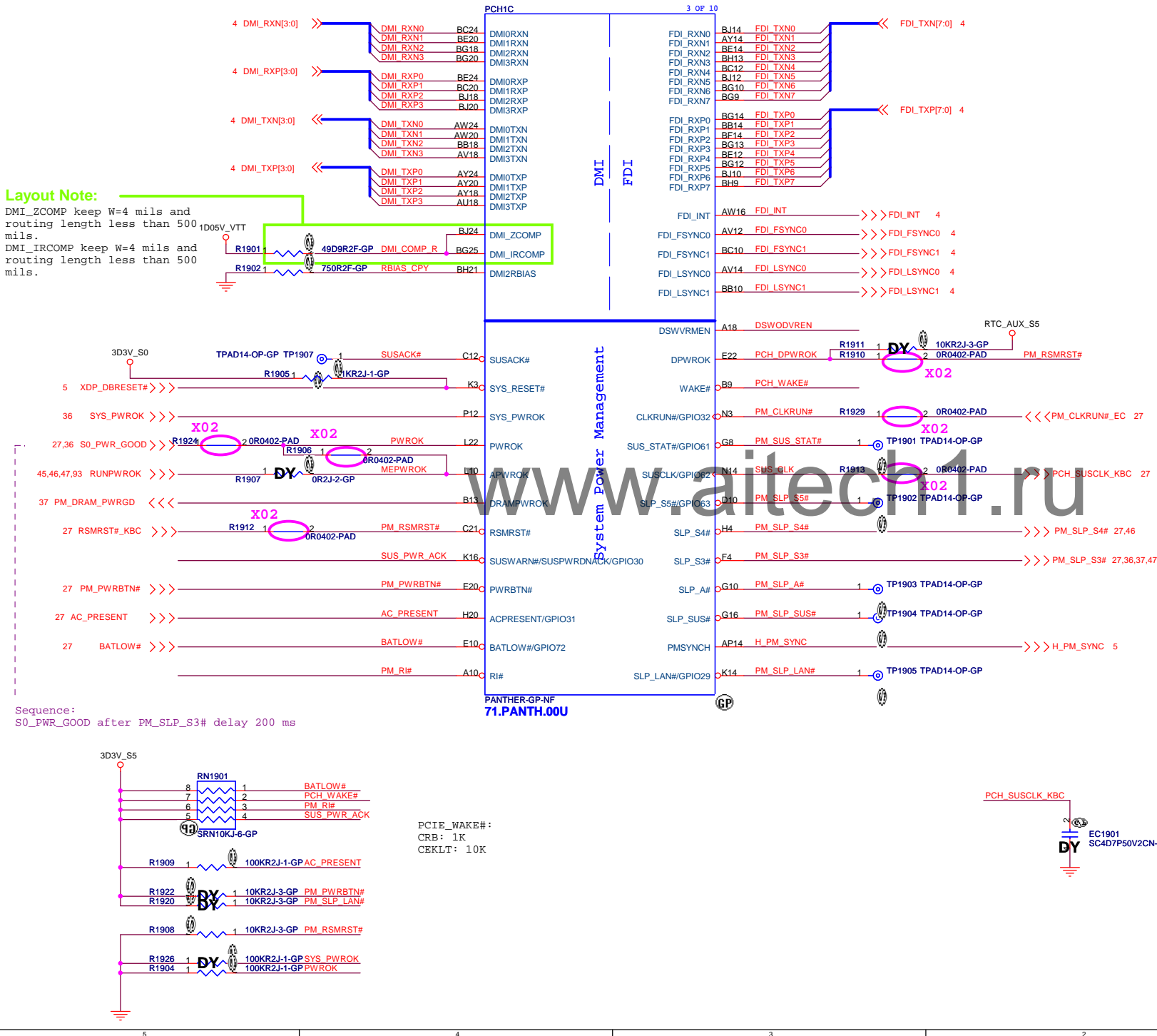
Sheet 18 of 104

X02

SSID = PCH

Layout Note:

```
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.
```



DSWQDVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5

DSWQDVREN R1917 330KR2J-L1-GP

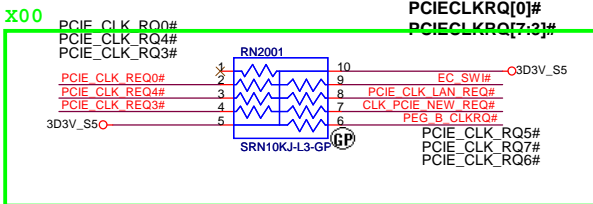


SSID = PCH

S5 power rail CLKREQ#:

PCIECLKRQ[0]#

PCIECLKRQ[7:3]#



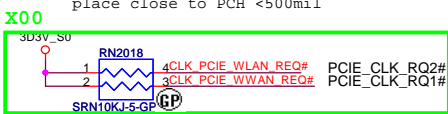
65 PCIE_RXN4
65 PCIE_RXP4
65 PCIE_TXN4
65 PCIE_TXP4

31 PCIE_RXN2
31 PCIE_RXP2
31 PCIE_TXN2
31 PCIE_TXP2

S0 power rail CLKREQ#:

PCIECLKRQ[2:1]#

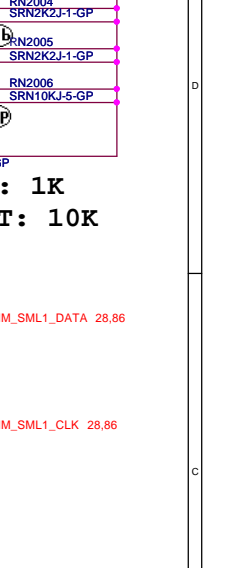
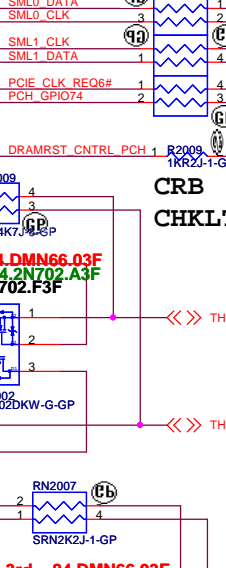
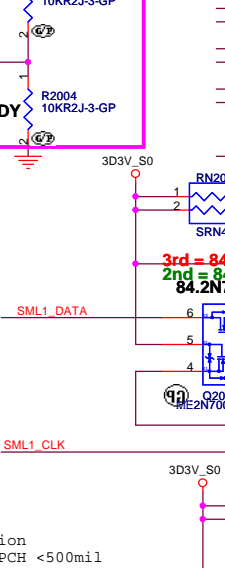
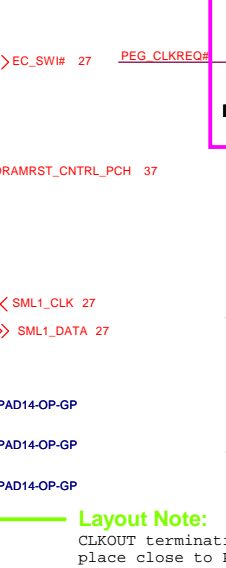
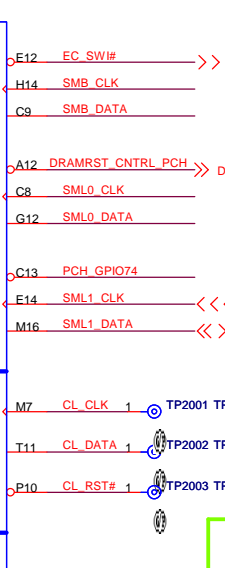
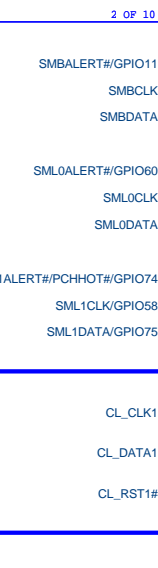
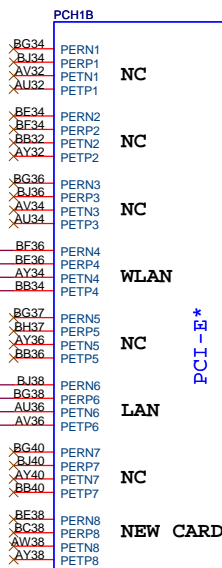
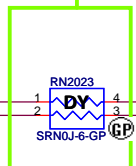
CLKOUT termination
place close to PCH <500mil



Layout Note:

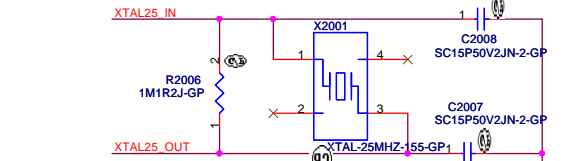
65 CLK_PCIE_WLAN#
65 CLK_PCIE_WLAN#
65 CLK_PCIE_WLAN_REQ#

31 CLK_PCIE_LAN#
31 CLK_PCIE_LAN#
31 PCIE_CLK_LAN_REQ#



Layout Note:

CLKOUT termination
place close to PCH <500mil

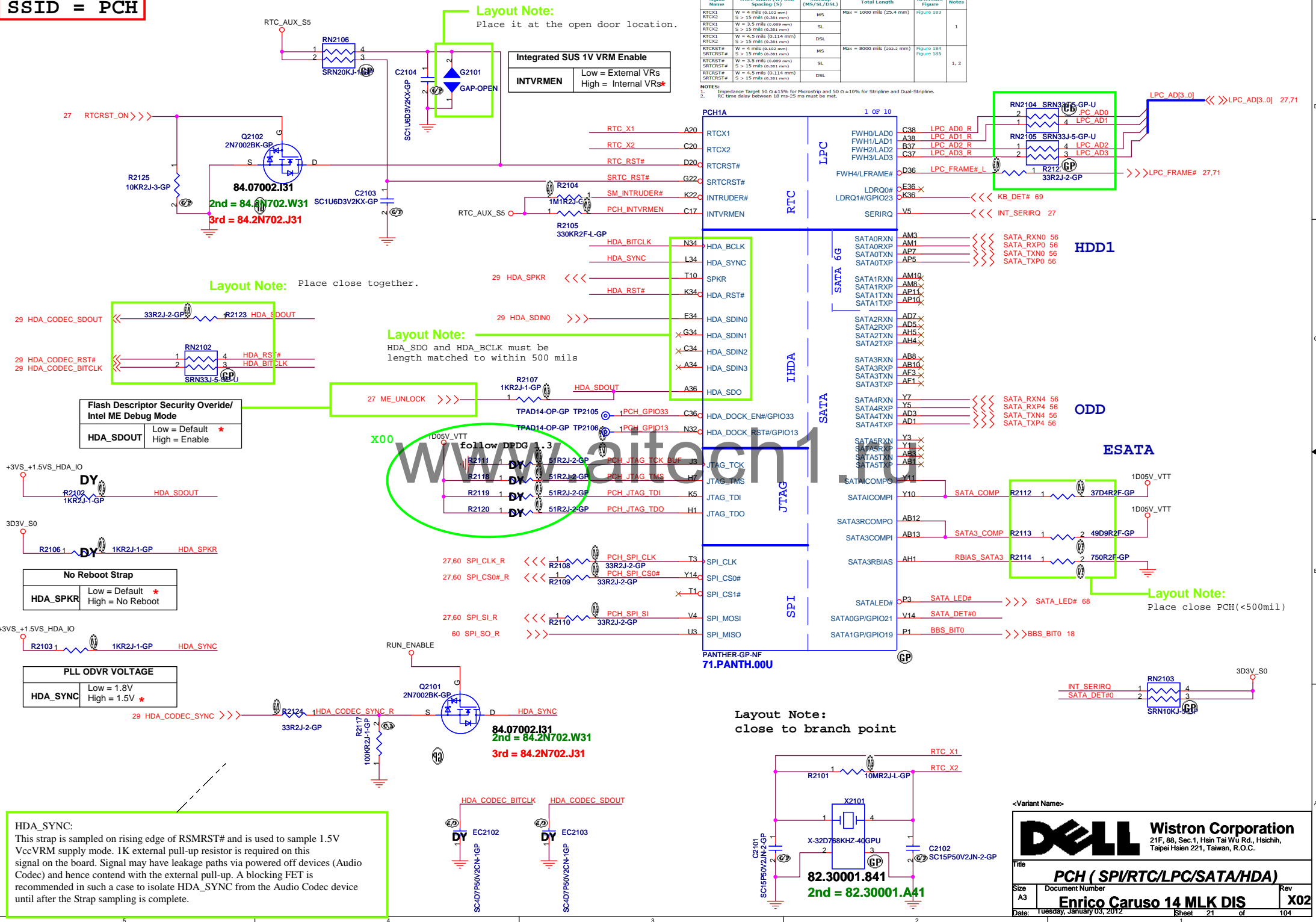


82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

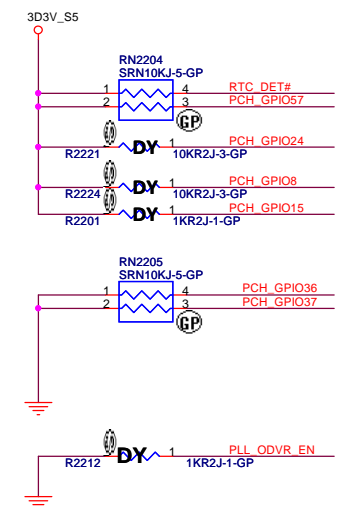
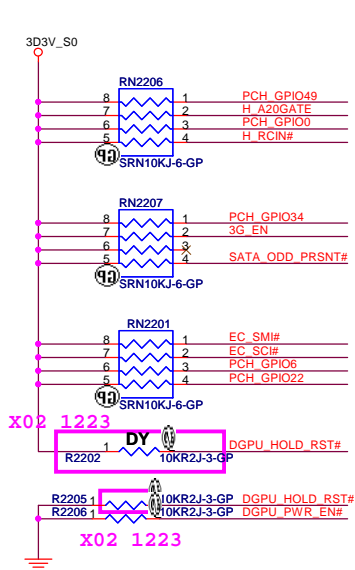
BIOS UMA/Discrete Strap pin		
	BOARD_ID1	BOARD_ID2
PX (AMD)	0	0
DIS	0	1
UMA	1	0
Optimus (NV)	1	1

DELL Wistron Corporation
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SSID = PCH



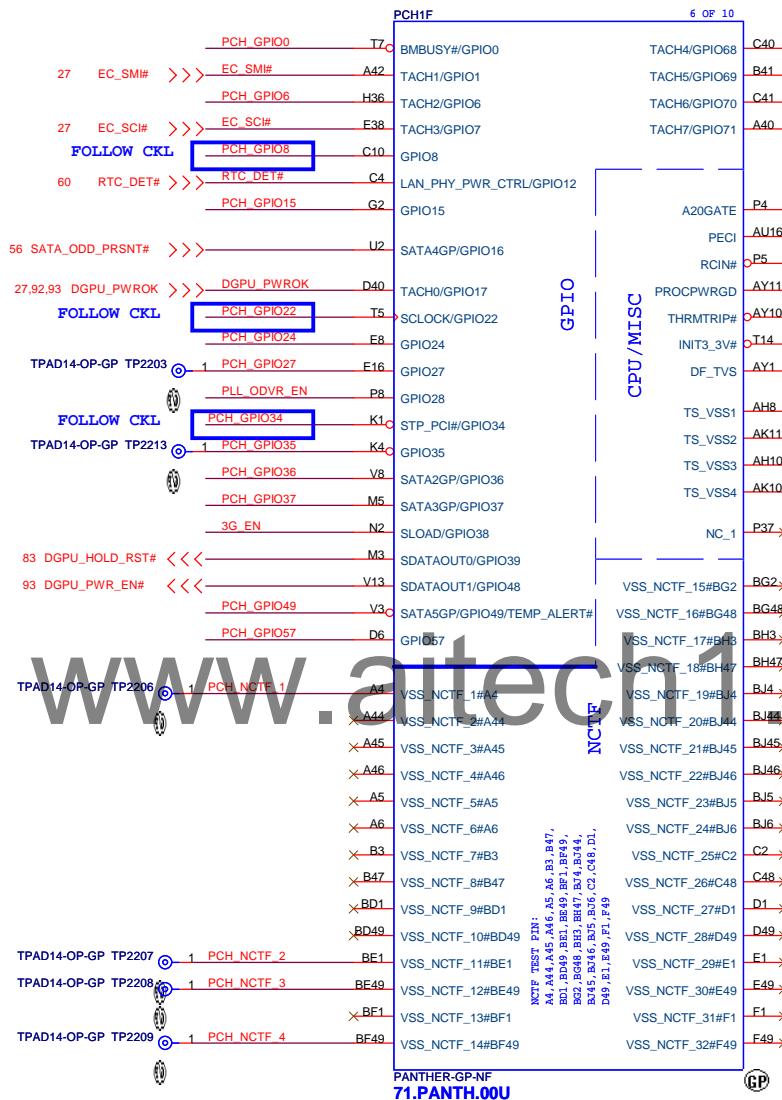
SSID = PCH



PLL ON DIE VR ENABLE

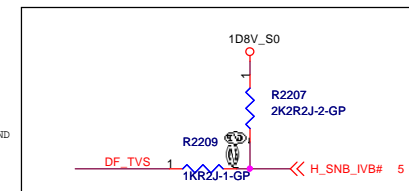
GPIO28
(PLL_ODVR_EN)

Weakly internal pull up 20k.
High - Enable
LOW - Disable



Layout Note:

These four balls must connect to GND
shared 1 Via



<Variant Name>



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Title

PCH (GPIO/CPU)

Size

Document Number

Enrico Caruso 14 MLK DIS

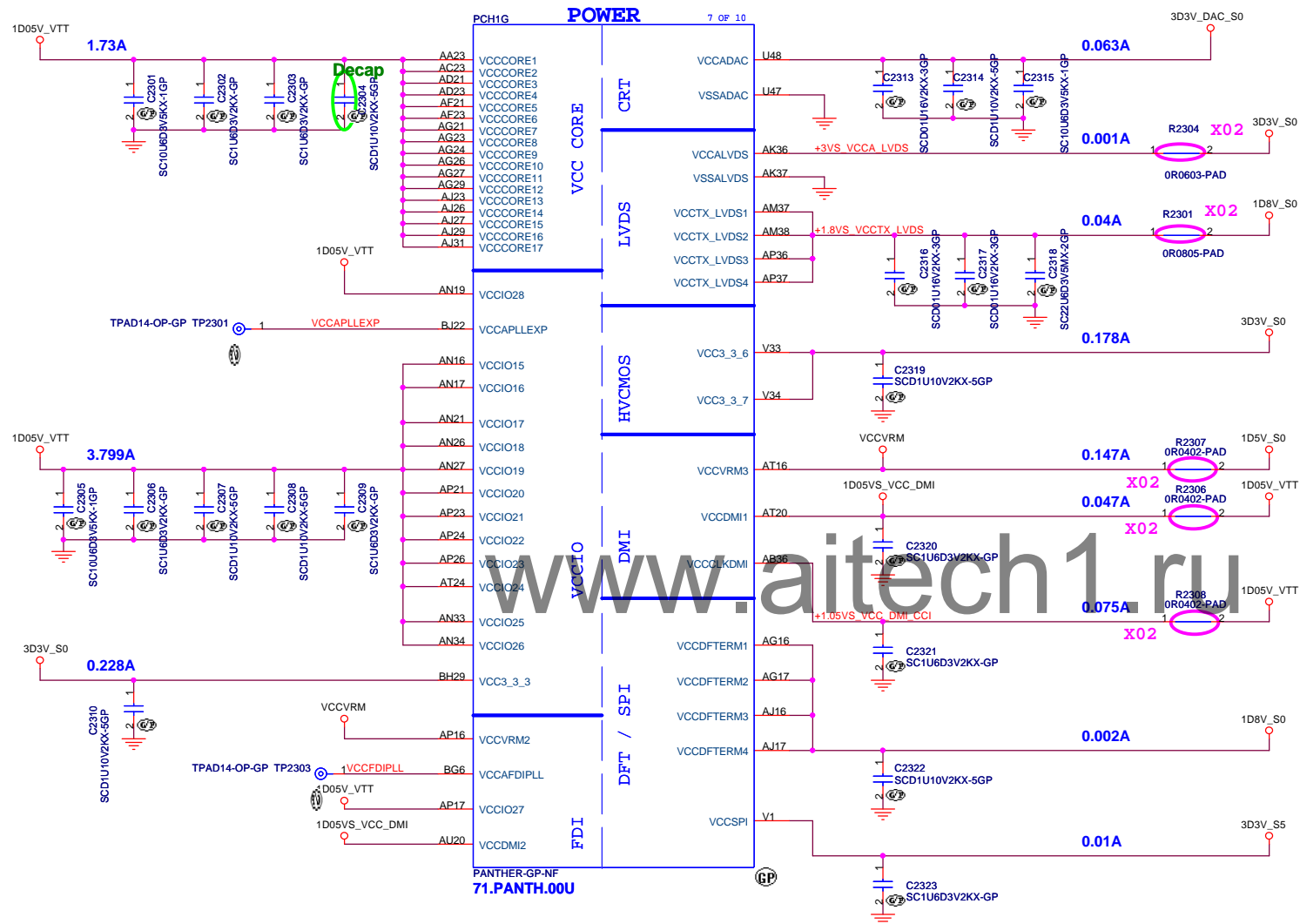
Rev

X02

Date: Tuesday, January 03, 2012

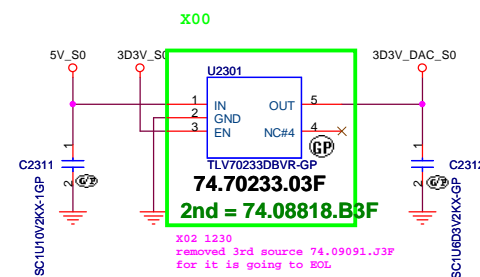
Sheet 22 of 104

SSID = PCH

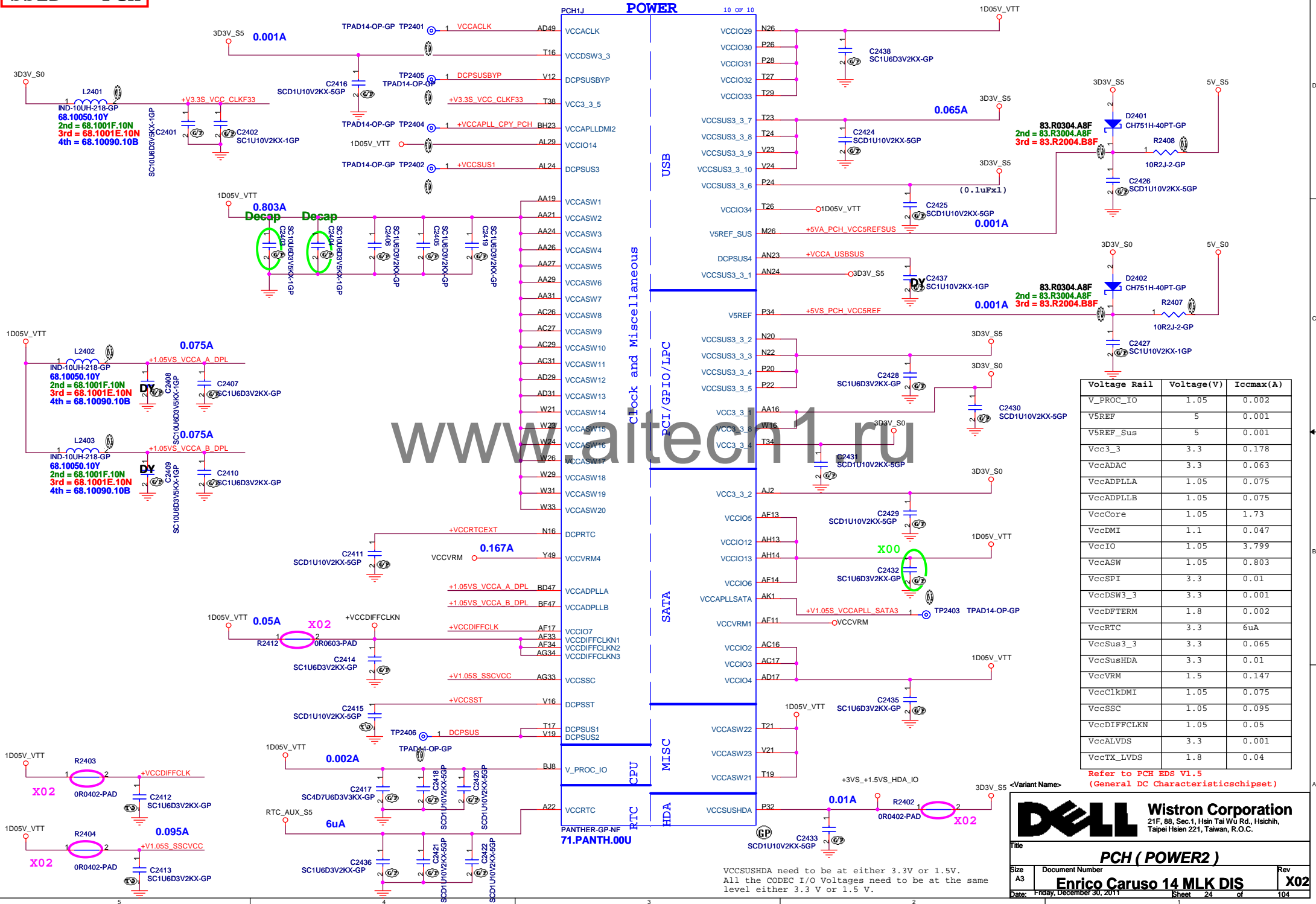


Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to PCH EDS V1.5
(General DC Characteristicschipset)



SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to PCH EDS V1.5
(General DC Characteristicschipset)



Title			
PCH (POWER2)			
Size	Document Number	Rev	
A3	Enrico Caruso 14 MLK DIS	X02	
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SSID = PCH

PCH1H 8 OF 10		
H5	VSS0	
AA17	VSS1	VSS80 AK38
AA2	VSS2	VSS81 AK4
AA3	VSS3	VSS82 AK42
AA33	VSS4	VSS83 AK46
AA34	VSS5	VSS84 AK8
AB11	VSS6	AL16
AB14	VSS7	VSS85 AL17
AB39	VSS8	VSS86 AL19
AB4	VSS9	VSS87 AL2
AB43	VSS10	VSS88 AL21
AB5	VSS11	VSS89 AL23
AB7	VSS12	VSS90 AL26
AC19	VSS13	VSS91 AL27
AC2	VSS14	VSS92 AL31
AC21	VSS15	VSS93 AL33
AC24	VSS16	VSS94 AL34
AC33	VSS17	VSS95 AL48
AC34	VSS18	VSS96 ALM1
AC48	VSS19	VSS97 AM14
AD10	VSS20	VSS98 AM36
AD11	VSS21	VSS99 AM39
AD12	VSS22	VSS100 AM43
AD13	VSS23	VSS101 AM45
AD19	VSS24	VSS102 AM46
AD24	VSS25	VSS103 AM7
AD26	VSS26	VSS104 AN2
AD27	VSS27	VSS105 AN29
AD33	VSS28	VSS106 AN3
AD34	VSS29	VSS107 AN31
AD36	VSS30	VSS108 AP12
AD37	VSS31	VSS109 AP19
AD38	VSS32	VSS110 AP28
AD39	VSS33	VSS111 AP30
AD4	VSS34	VSS112 AP32
AD40	VSS35	VSS113 AP38
AD42	VSS36	VSS114 AP4
AD43	VSS37	VSS115 AP42
AD45	VSS38	VSS116 AP46
AD46	VSS39	VSS117 AP8
AD8	VSS40	VSS118 AR2
AE2	VSS41	VSS119 AR48
AE3	VSS42	VSS120 AT11
AE10	VSS43	VSS121 AT13
AE12	VSS44	VSS122 AT18
AD14	VSS45	VSS123 AT22
AD16	VSS46	VSS124 AT26
AE16	VSS47	VSS125 AT28
AF19	VSS48	VSS126 AT30
AF24	VSS49	VSS127 AT32
AF26	VSS50	VSS128 AT34
AF27	VSS51	VSS129 AT39
AF29	VSS52	VSS130 AT42
AF31	VSS53	VSS131 AT46
AF38	VSS54	VSS132 AT7
AF4	VSS55	VSS133 AU24
AF42	VSS56	VSS134 AU30
AF46	VSS57	VSS135 AU36
AF5	VSS58	VSS136 AV20
AF7	VSS59	VSS137 AV24
AF8	VSS60	VSS138 AV30
AG19	VSS61	VSS139 AV38
AG2	VSS62	VSS140 AV4
AG31	VSS63	VSS141 AV43
AG48	VSS64	VSS142 AV8
AH11	VSS65	VSS143 AW14
AH3	VSS66	VSS144 AW18
AH36	VSS67	VSS145 AW2
AH39	VSS68	VSS146 AW22
AH40	VSS69	VSS147 AW26
AH42	VSS70	VSS148 AW28
AH46	VSS71	VSS149 AW32
AH7	VSS72	VSS150 AW34
AJ19	VSS73	VSS151 AW36
AJ21	VSS74	VSS152 AW40
AJ24	VSS75	VSS153 AW48
AJ33	VSS76	VSS154 AW11
AJ34	VSS77	VSS155 AY12
AK12	VSS78	VSS156 AY22
AK3	VSS79	VSS157 AY28
		VSS158

PANTHER-GP-NF
71.PANTH.00U



PCH1I 9 OF 10

AY4	VSS159	VSS259 H46
AY42	VSS160	VSS260 K18
AY46	VSS161	VSS261 K26
B11	VSS162	VSS262 K39
B15	VSS163	VSS263 K46
B19	VSS164	VSS264 K7
B23	VSS165	VSS265 L18
B27	VSS166	VSS266 L2
B31	VSS167	VSS267 L20
B35	VSS168	VSS268 L26
B39	VSS169	VSS269 L28
B7	VSS170	VSS270 L36
F45	VSS171	VSS271 L48
BB12	VSS172	VSS272 M12
BB16	VSS173	VSS273 P16
BB20	VSS174	VSS274 M18
BB22	VSS175	VSS275 M22
BB24	VSS176	VSS276 M24
BB28	VSS177	VSS277 M30
BB30	VSS178	VSS278 M32
BB38	VSS179	VSS279 M34
BB4	VSS180	VSS280 M38
BB46	VSS181	VSS281 M4
BC14	VSS182	VSS282 M42
BC18	VSS183	VSS283 M46
BC2	VSS184	VSS284 M8
BC22	VSS185	VSS285 N18
BC26	VSS186	VSS286 P30
BC32	VSS187	VSS287 N47
BC34	VSS188	VSS288 P11
BC36	VSS189	VSS289 P18
BC40	VSS190	VSS290 T33
BC42	VSS191	VSS291 P40
BC48	VSS192	VSS292 P43
BD46	VSS193	VSS293 P47
BD5	VSS194	VSS294 P7
BE22	VSS195	VSS295 R2
BE26	VSS196	VSS296 R48
BE40	VSS197	VSS297 T12
BF10	VSS198	VSS298 T31
BF12	VSS199	VSS299 T37
BF16	VSS200	VSS300 T4
BF20	VSS201	VSS301 W34
BF22	VSS202	VSS302 T46
BF24	VSS203	VSS303 T47
BF26	VSS204	VSS304 T8
BF28	VSS205	VSS305 V11
BF3	VSS206	VSS306 V17
BF38	VSS207	VSS307 V26
BF40	VSS208	VSS308 V27
BF42	VSS209	VSS309 V29
BF46	VSS210	VSS310 V31
BG17	VSS211	VSS311 V36
BG24	VSS212	VSS312 V39
BG33	VSS213	VSS313 V43
BG44	VSS214	VSS314 V7
BG8	VSS215	VSS315 W17
BH11	VSS216	VSS316 W19
BH15	VSS217	VSS317 W2
BH17	VSS218	VSS318 W27
BH19	VSS219	VSS319 W48
H10	VSS220	VSS320 Y12
BH27	VSS221	VSS321 Y38
BH31	VSS222	VSS322 Y4
BH33	VSS223	VSS323 Y42
BH35	VSS224	VSS324 Y46
BH39	VSS225	VSS325 Y8
BH43	VSS226	VSS326 BG29
BH7	VSS227	VSS327 N24
D3	VSS228	VSS328 AJ3
D12	VSS229	VSS329 AD47
D16	VSS230	VSS330 B43
D18	VSS231	VSS331 BE10
D22	VSS232	VSS332 BG41
D24	VSS233	VSS333 G14
D26	VSS234	VSS334 H16
D30	VSS235	VSS335 T36
D32	VSS236	VSS336 BG22
D34	VSS237	VSS337 BG24
D38	VSS238	VSS338 C22
D42	VSS239	VSS339 AP13
D46	VSS240	VSS340 M14
E18	VSS241	VSS341 AP3
E26	VSS242	VSS342 AP1
G18	VSS243	VSS343 BE16
G20	VSS244	VSS344 BC16
G26	VSS245	VSS345 BG28
G28	VSS246	VSS346 BJ28
G36	VSS247	
G48	VSS248	
H12	VSS249	
H18	VSS250	
H22	VSS251	
H24	VSS252	
H26	VSS253	
H30	VSS254	
H32	VSS255	
H34	VSS256	
F3	VSS257	
	VSS258	

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71.PANTH.00U



<Variant Name>



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Title PCH (VSS)		
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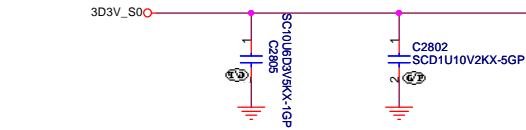
Title

Reserved

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SSID = Thermal

Thermal sensor NCT7718W

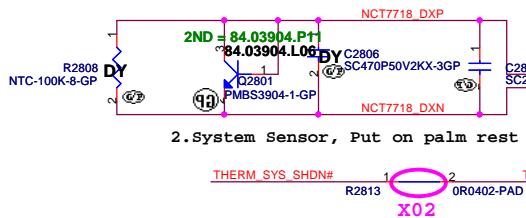


ALERT# /T CRIT#
Pull-up Resistor

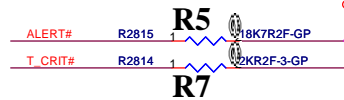
R5	77°C	87°C	97°C	107°C	117°C
2Kohm	79°C	89°C	99°C	109°C	119°C
7.5Kohm	81°C	91°C	101°C	111°C	121°C
10.5Kohm	83°C	93°C	103°C	113°C	123°C
14Kohm	85°C	95°C	105°C	115°C	125°C
18.7Kohm					

T_CRIT temperature strapping point

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing, and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W

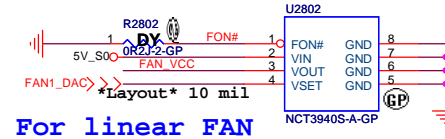


X02



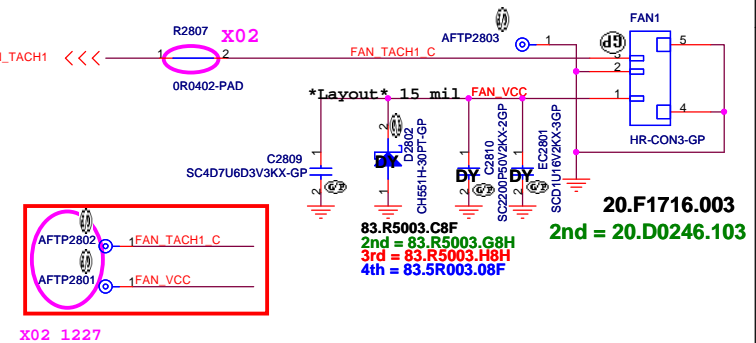
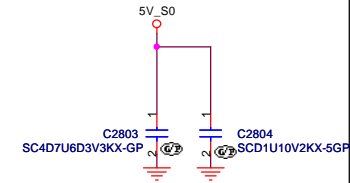
R7

Fan controller G991



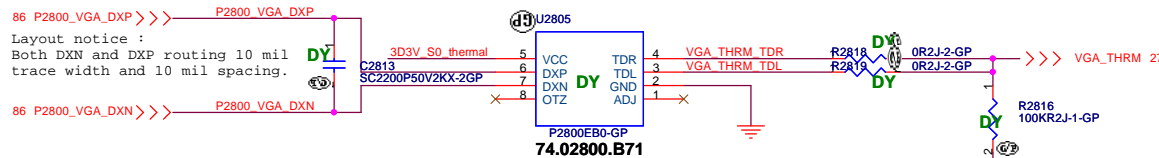
For linear FAN

74.03940.A71
2nd = 74.02793.A31
3rd = 74.00991.031

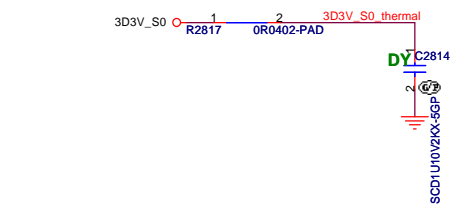


X02 1227

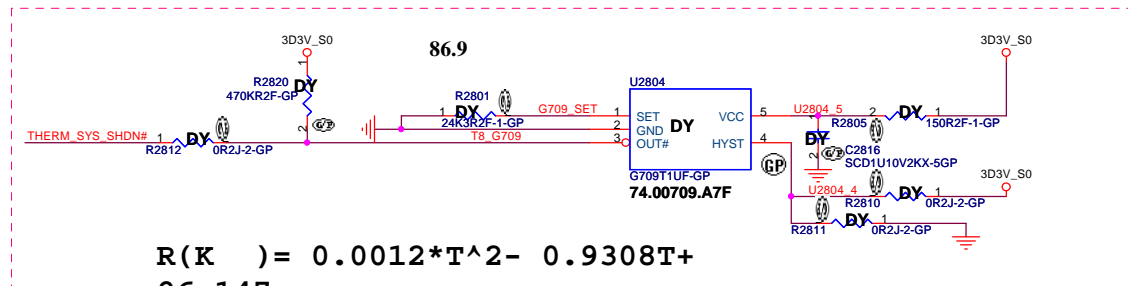
VGA Thermal sensor P2800



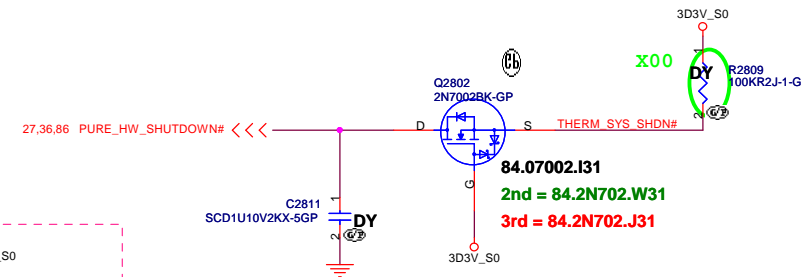
X02-0311 Add R2816& R2817 to
option VGA_THRM
and DY the circuit



86.9

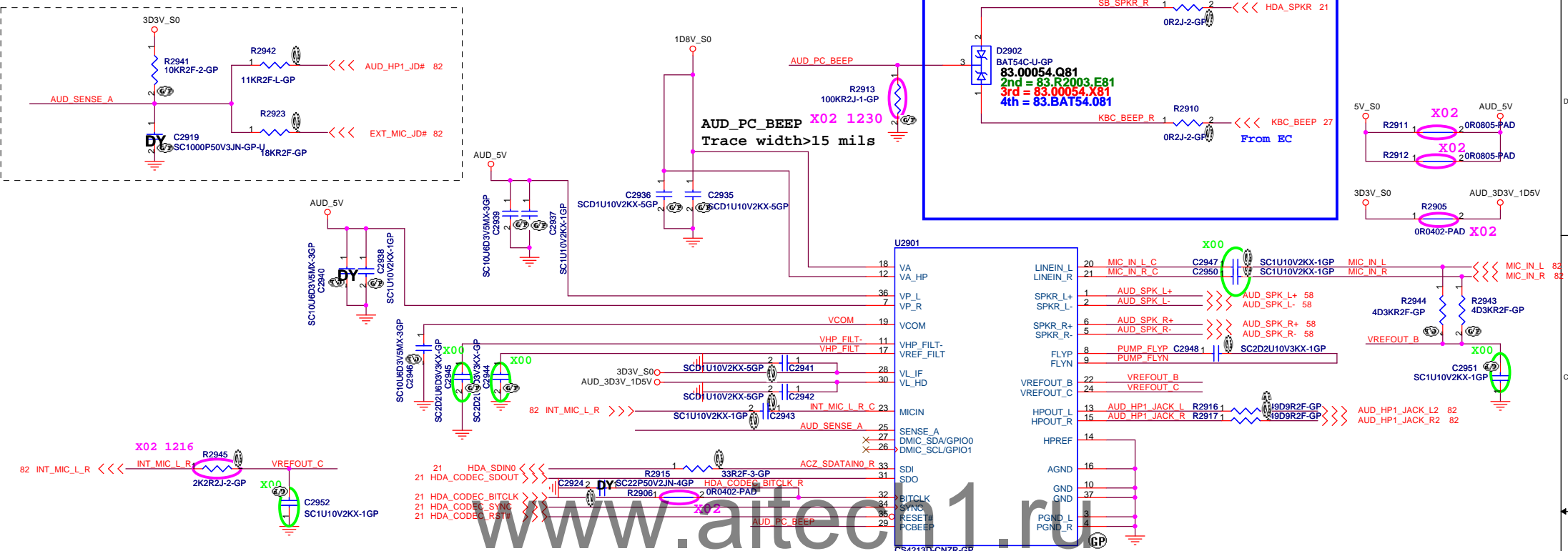


$$R(K) = 0.0012 * T^2 - 0.9308T + 96.147$$

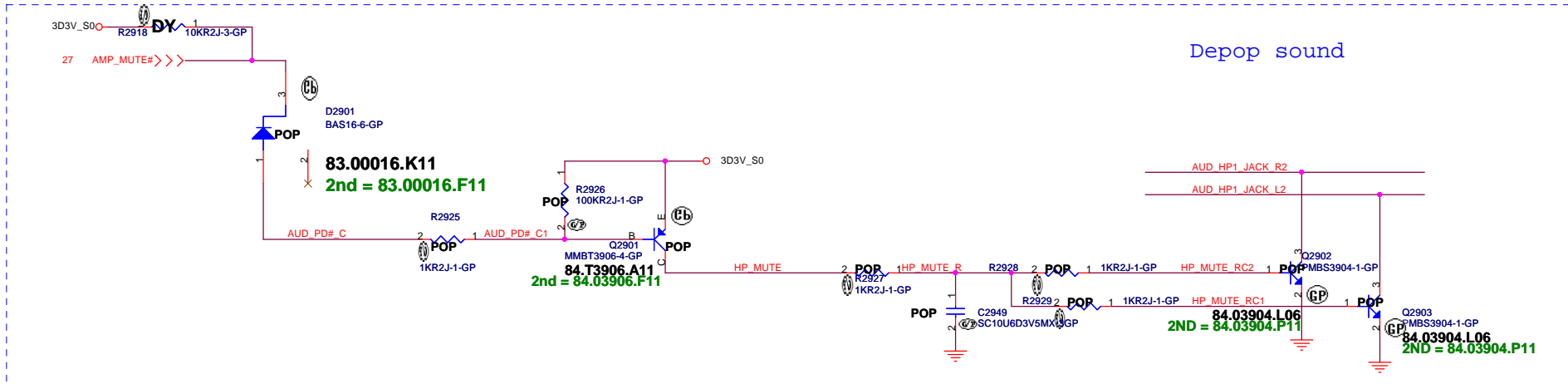


84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

SSID = AUDIO



71.04213.003



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Title

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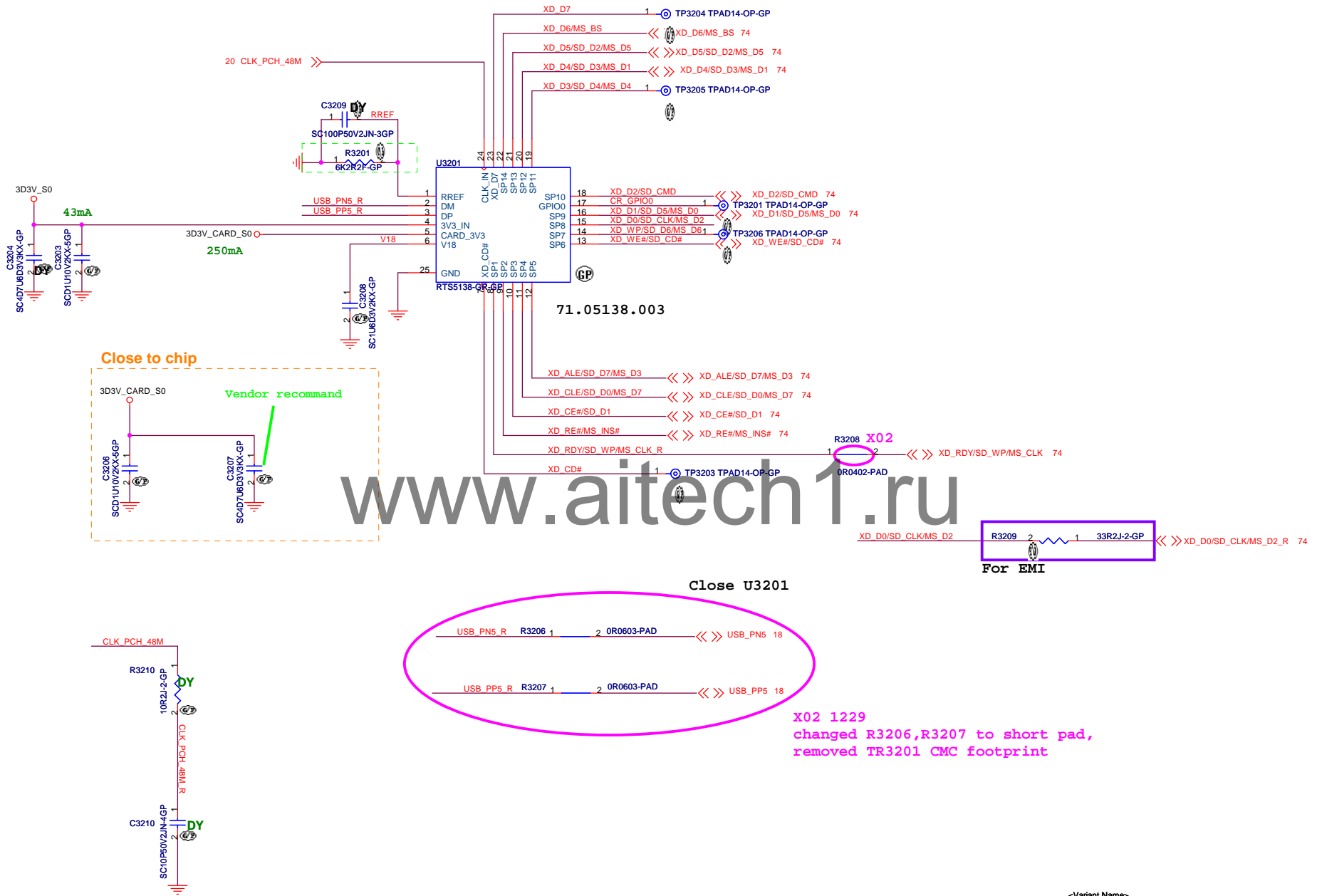
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
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RT81411F CGT GP



SSID = SDIO



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Title

Reserved

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<Variant Name>



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Title

Size
A3

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Enrico Caruso 14 MLK DIS

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Rev
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Reserved

(Blanking)

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<Variant Name>



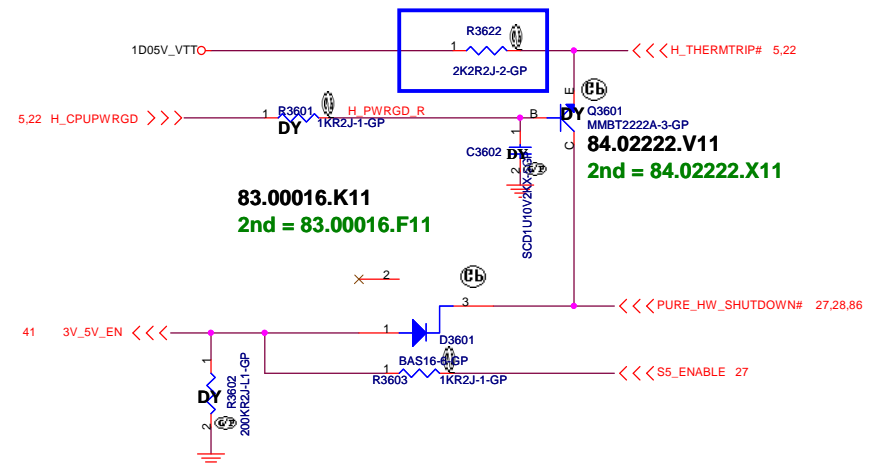
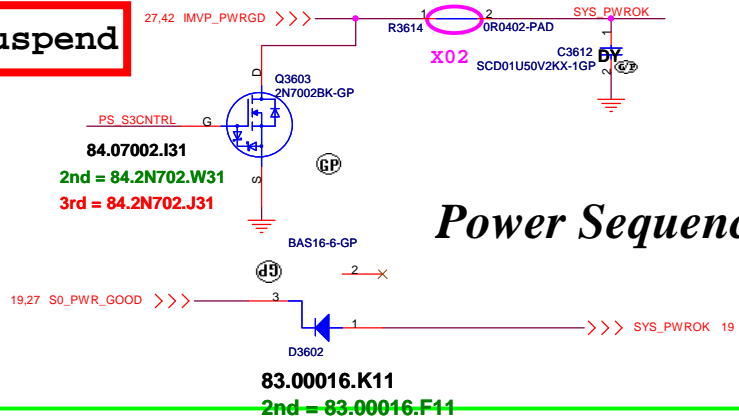
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

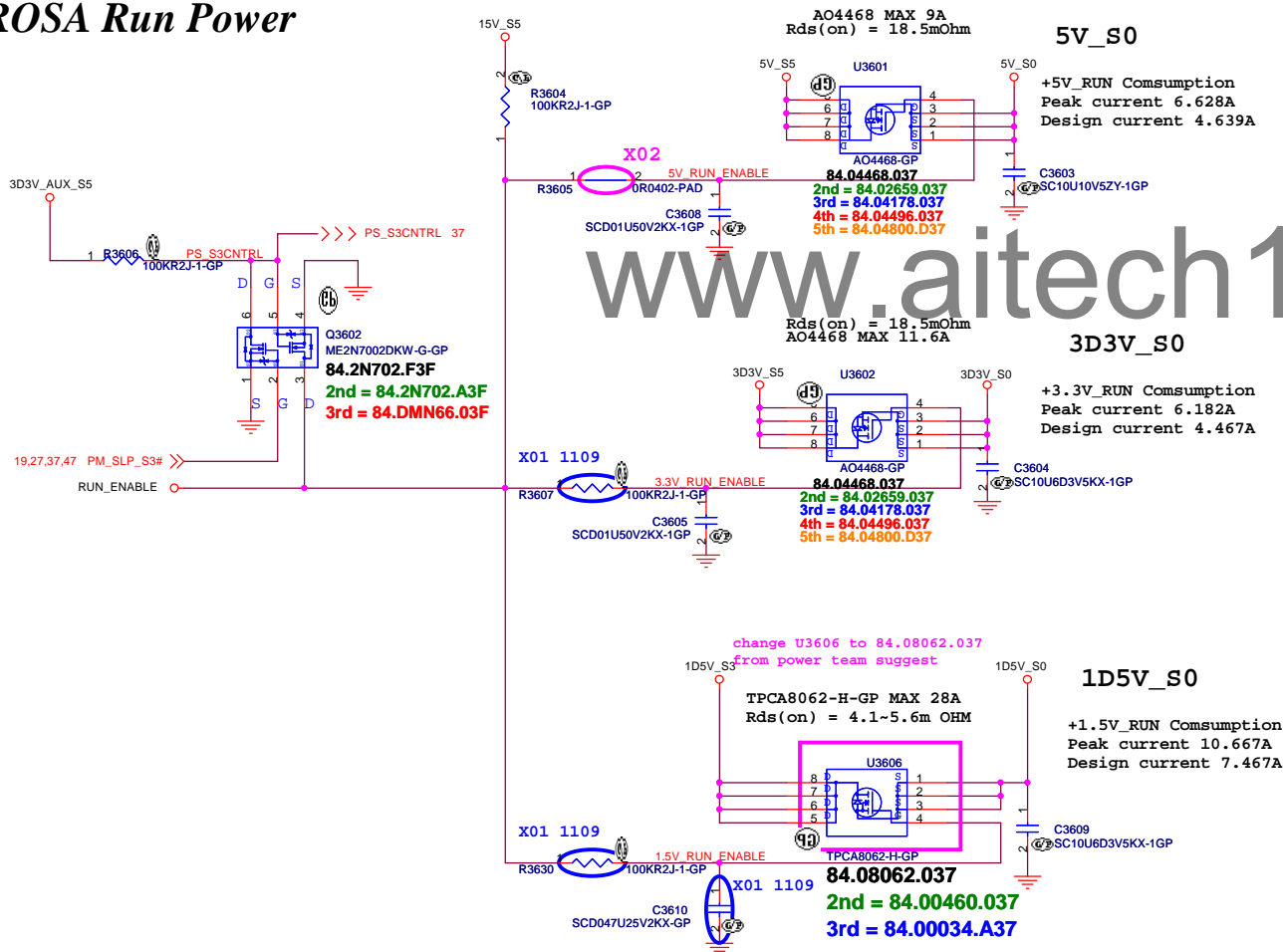
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Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 35 of 104	

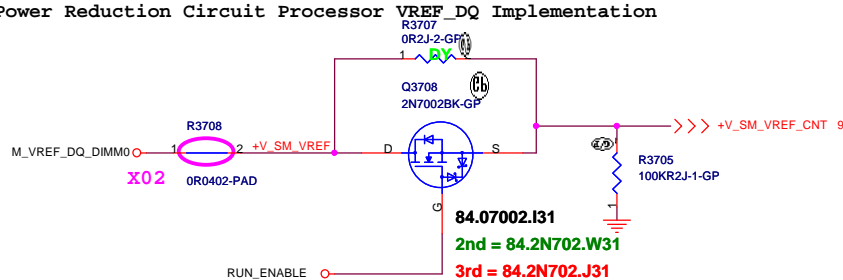
SSID = Reset.Suspend



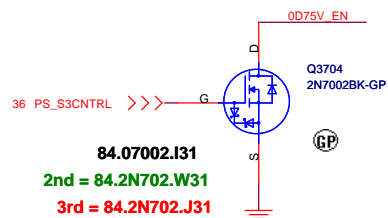
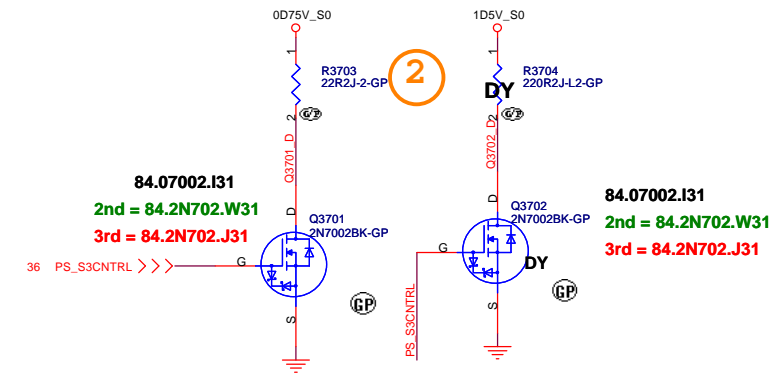
ROSA Run Power



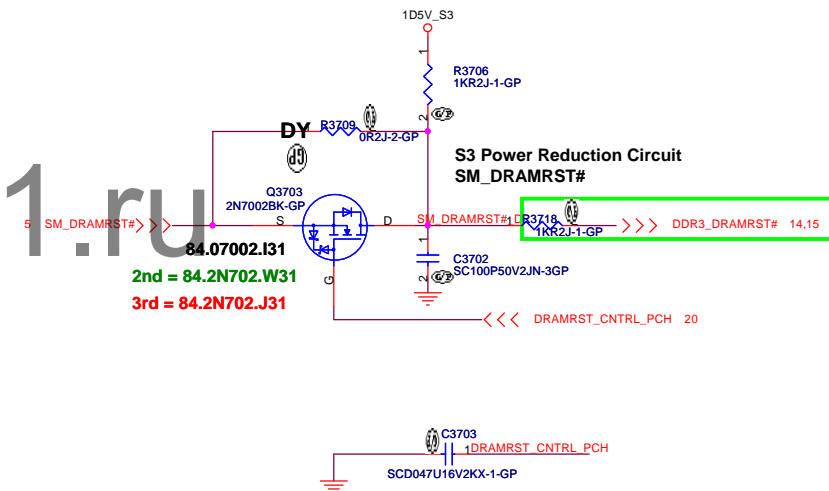
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

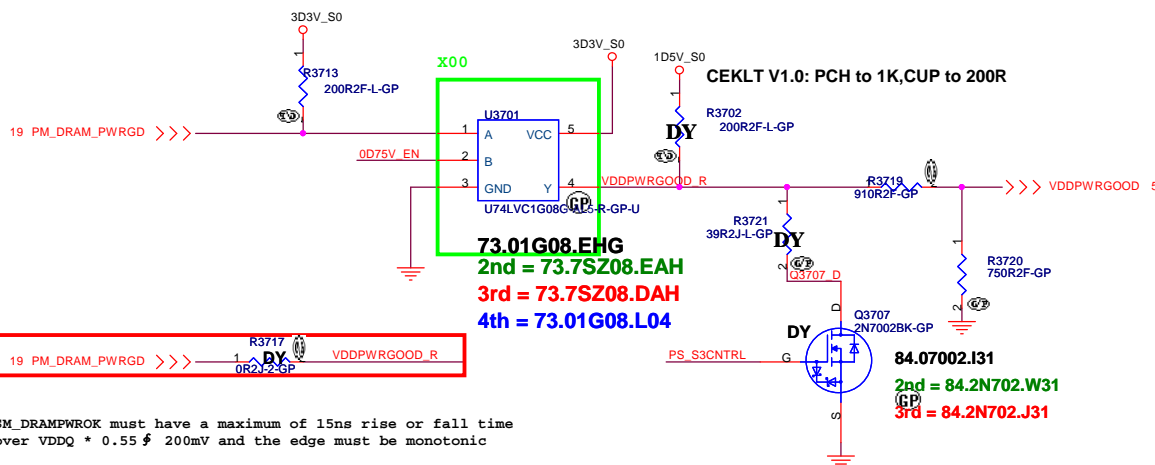


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



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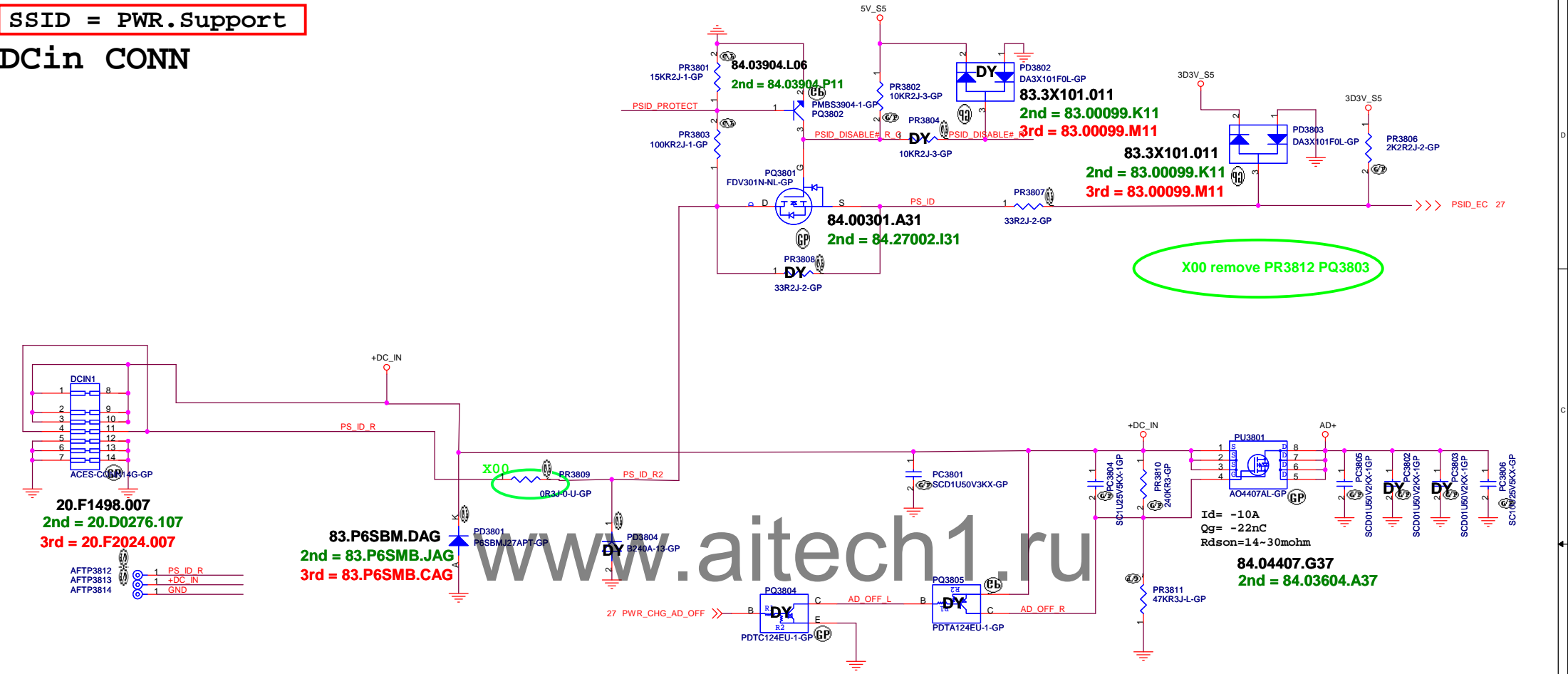
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 f 200mV and the edge must be monotonic

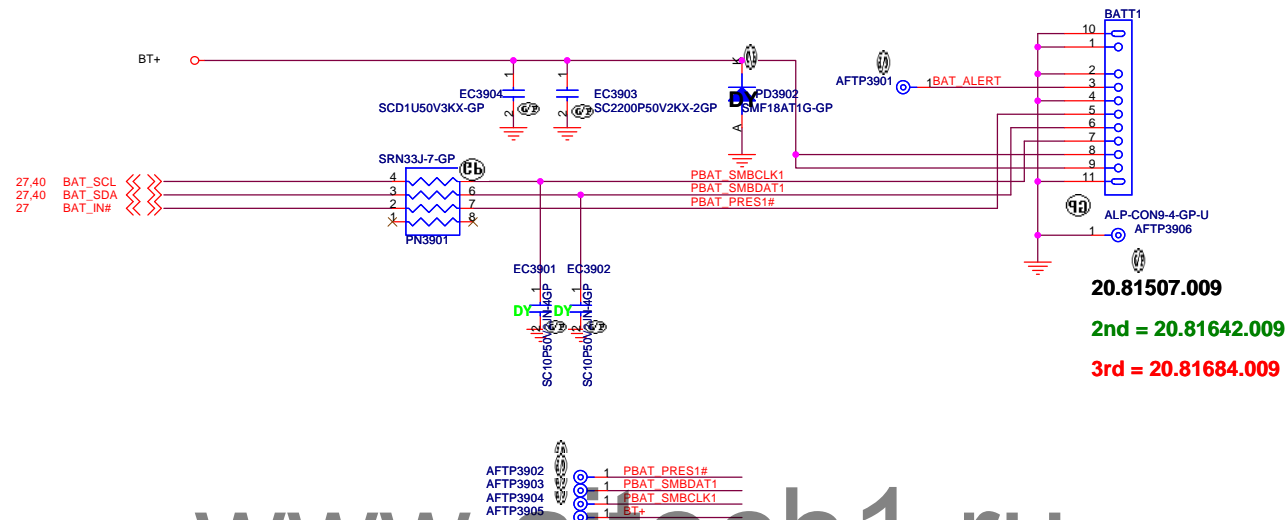
SSID = PWR.Support

DCin CONN



```
SSID = PWR.Support
```

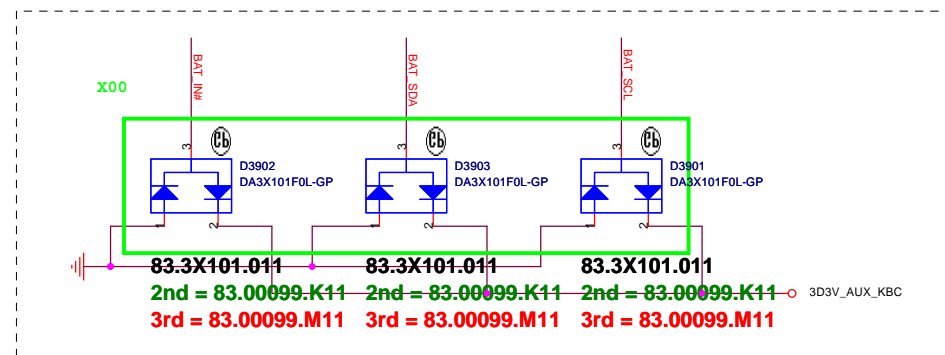
Batt Connector



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For actual location, need to be swap all pin

Placement: Close to Batt Connector

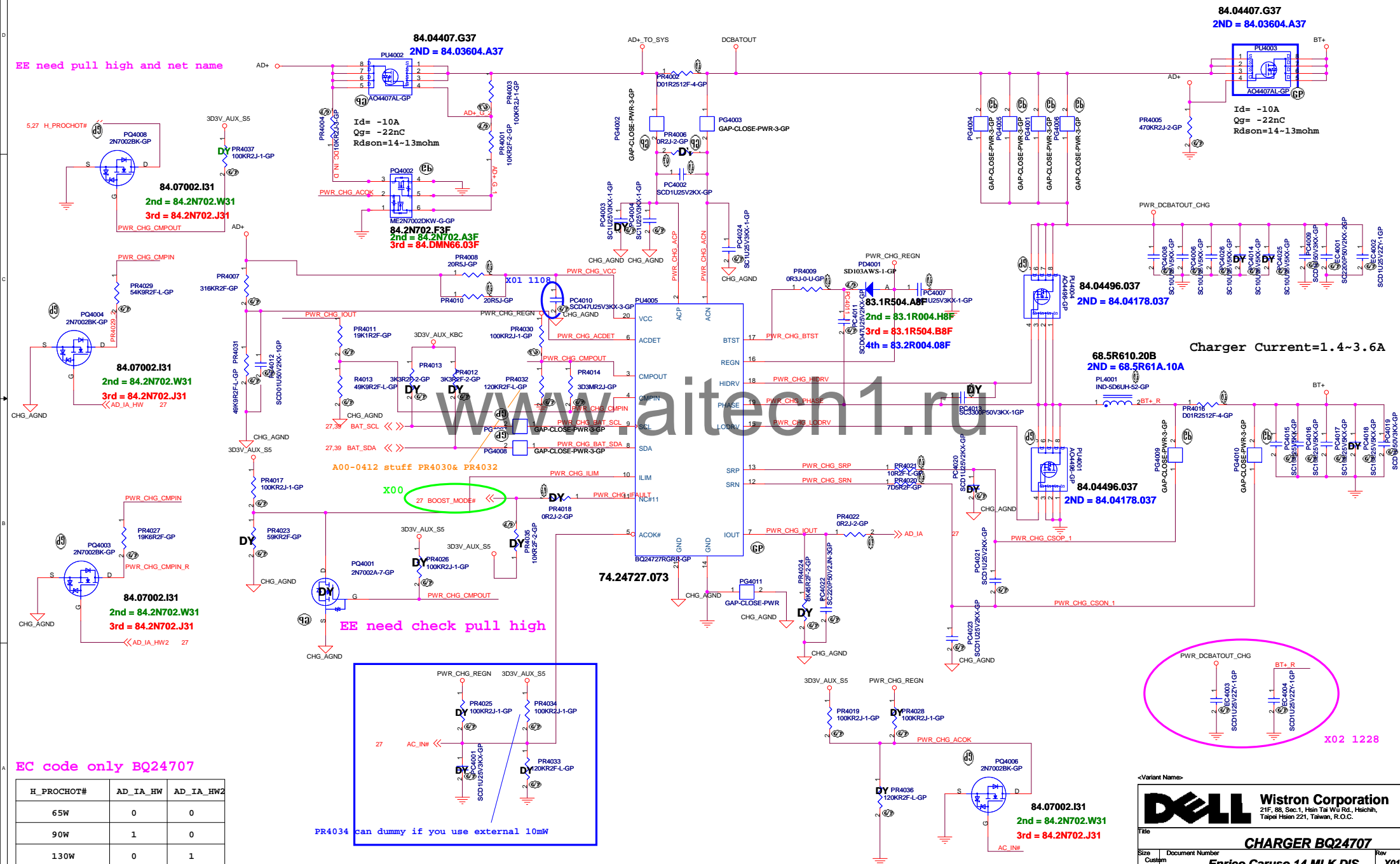


<Variant Name>



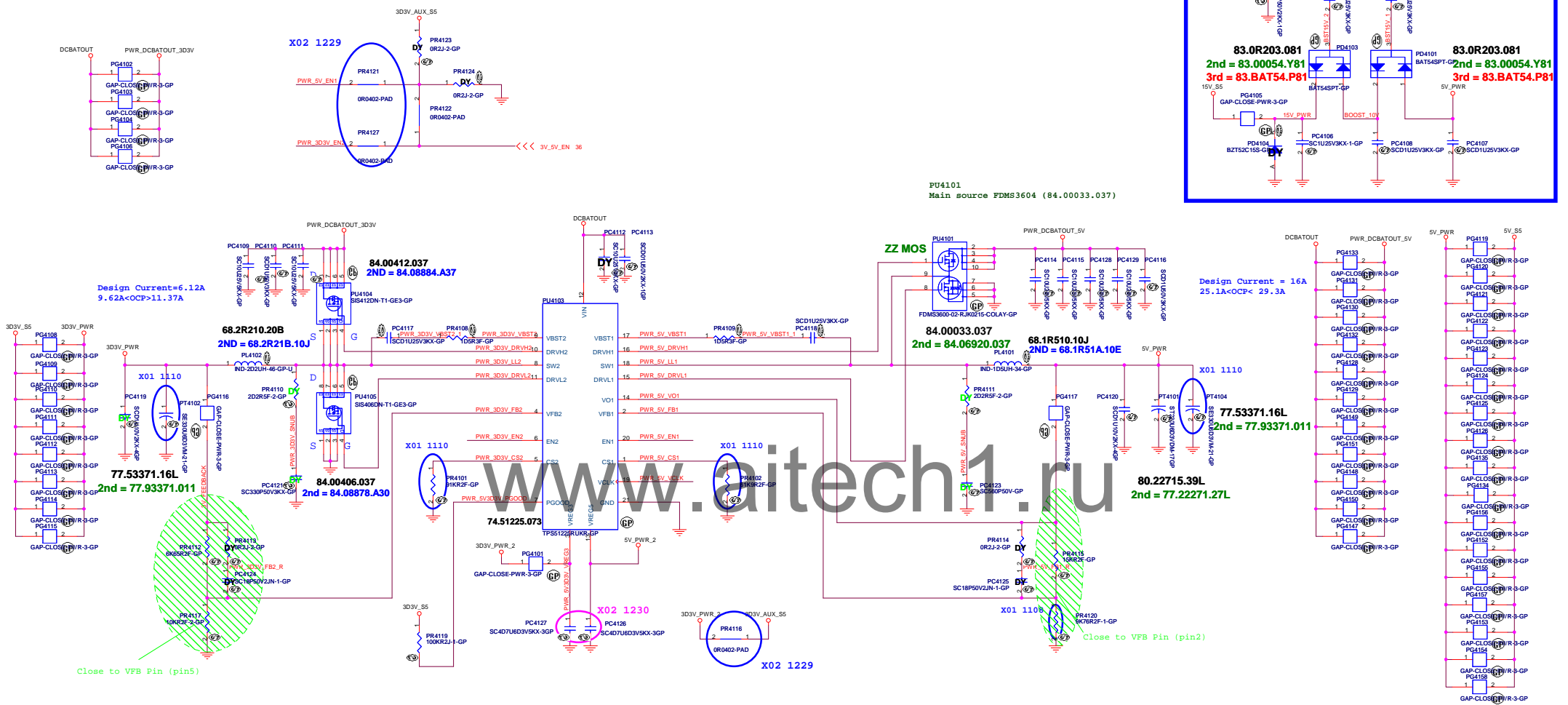
Title			
BATT CONN			
Size A3	Document Number Enrico Caruso 14 MLK DIS		Rev X01
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SSID = Charger



H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S: SIS412DN-T1-GE3 / 24mohm/30mohm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3 / 13.5mohm/16.5mohm@4.5Vgs / 84.07716.037

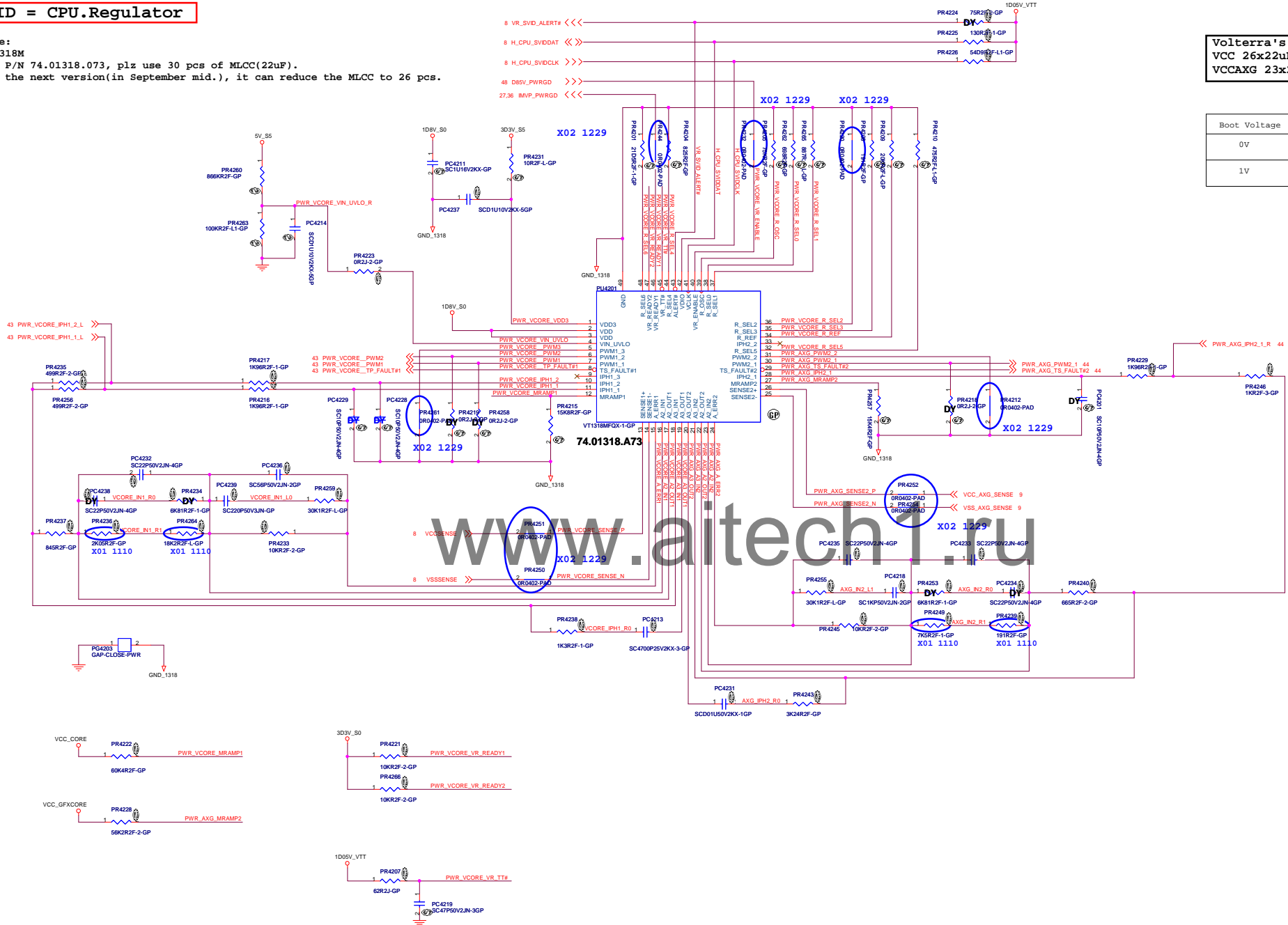
I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 6.3V PS1U01227M 25mohm 2.236Arms NEC TOKIN/77.C2271.00L
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S,L/S: FDMS3604S / 7.5mohm/9.8mohm@4.5Vgs, 2.6mohm/3.2mohm@4.5Vgs/ 84.03604.037

```
SSID = CPU.Regulator
```

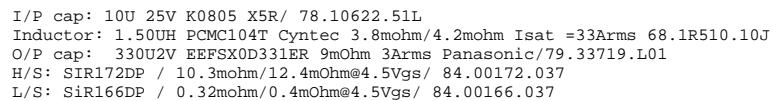
Note:
VT1318M
For P/N 74.01318.073, plz use 30 pcs of MLCC(22uF).
For the next version(in September mid.), it can reduce the MLCC to 26 pcs.

Volterra's suggestion:
VCC 26x22uF for 2-PHASE VCC
VCCAXG 23x22uF for 1-PHASE VCCAXG

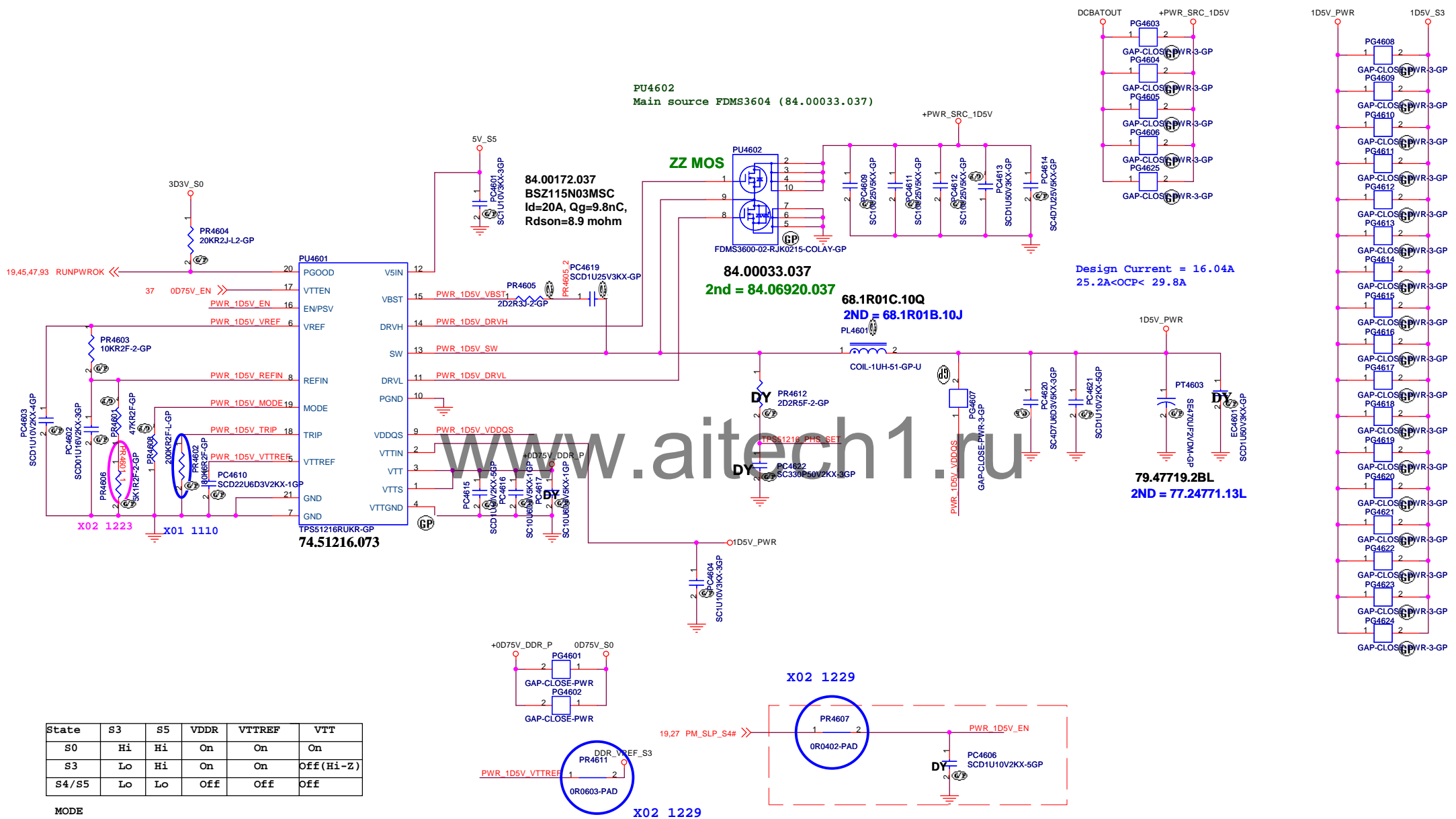
Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm



TPS51219 for 1D05V_PCH/VCCP_CPU



```
SSID = PWR.Plane.Regulator 1p5v0p75v
```



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

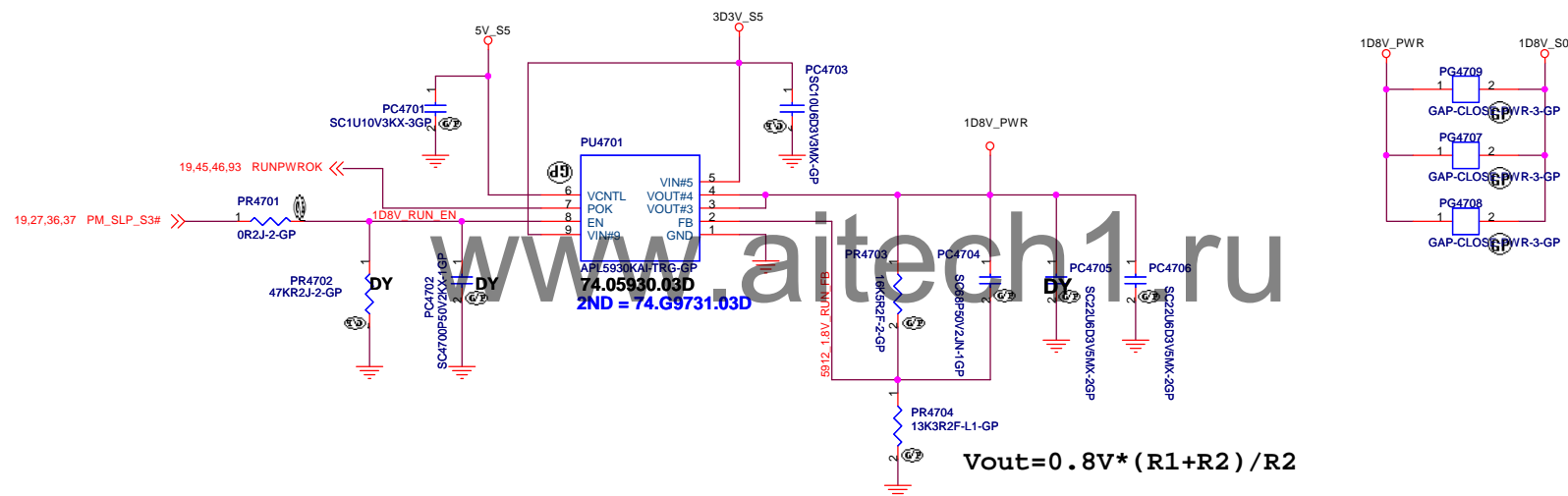
MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M Cyntec 3mohm/3.3mohm Isat =28Arms68.1R01C.10Q
O/P cap: CHIP CAP 470UF 2V EEFSXD471X 6mOhm 3.5Arm/Panasonic/79.47719.2BL
H/S,L/S: FDM53604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

SSID = PWR.Plane.Regulator_1p8v

APL5930 for 1D8V_S0

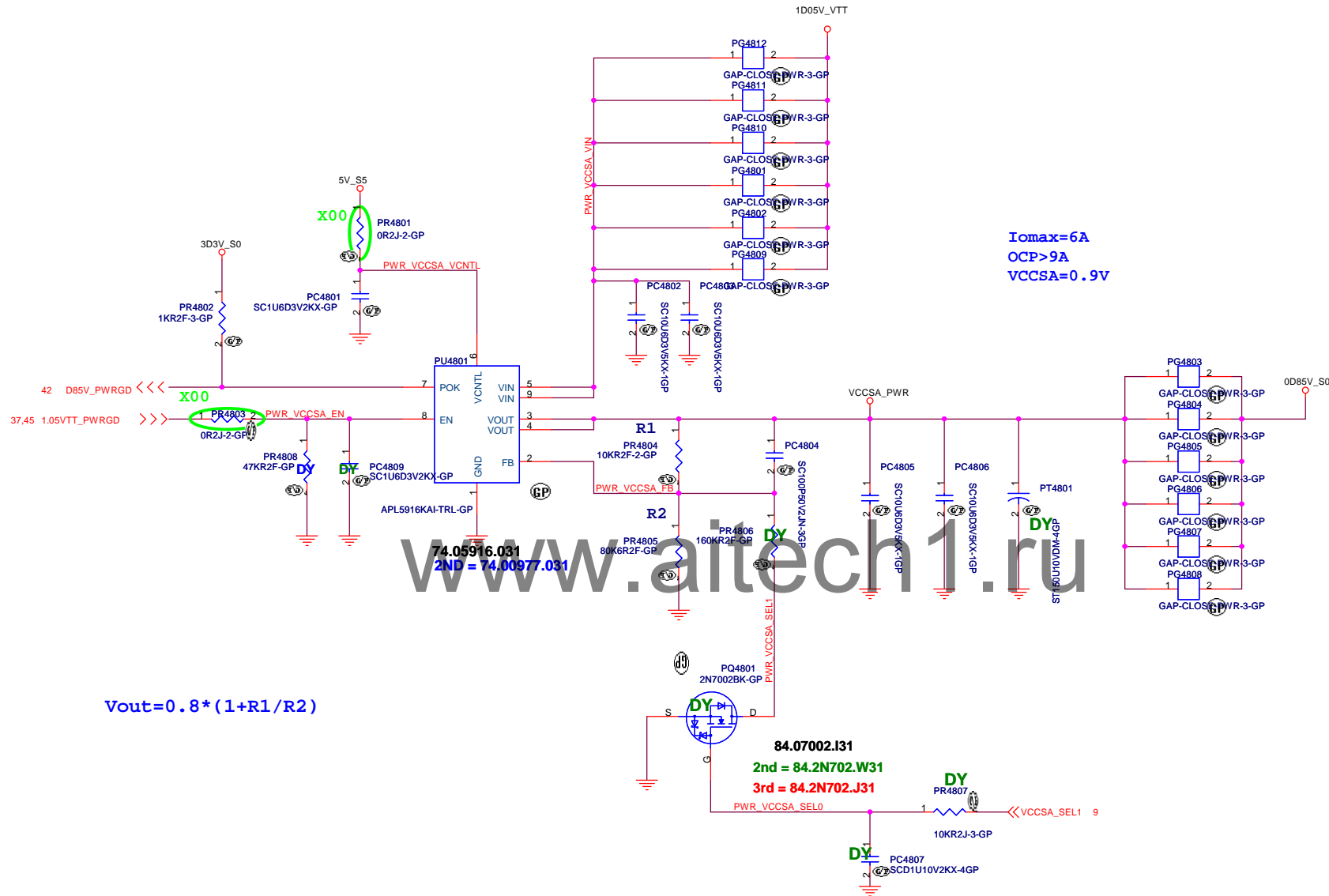
+1.8V_RUN
Design current = 1.086A



<Variant Name>

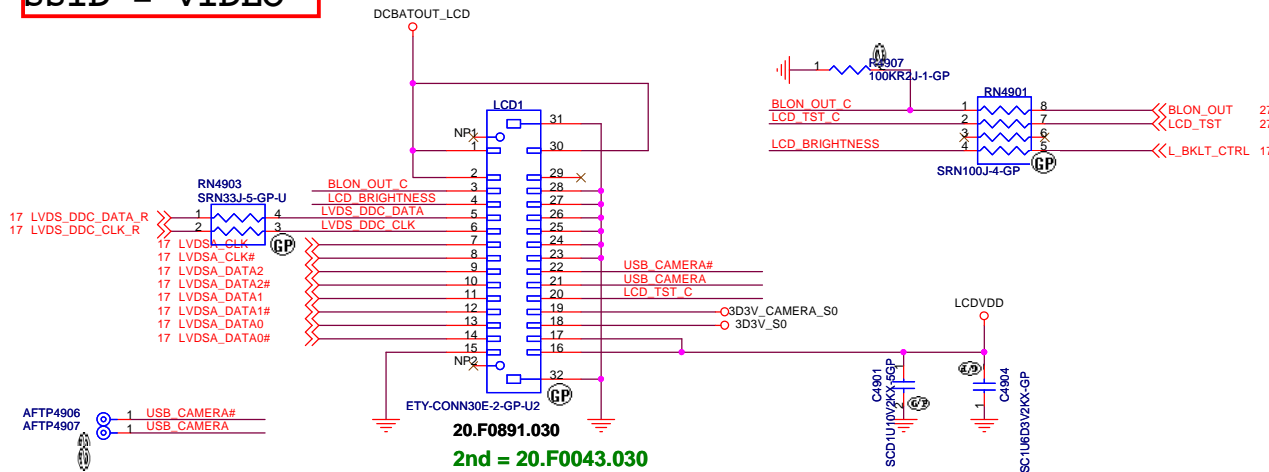
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title APL5930 1D8V S0			
Size A3	Document Number Enrico Caruso 14 MLK DIS		Rev X01
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APL5916 for VCCSA



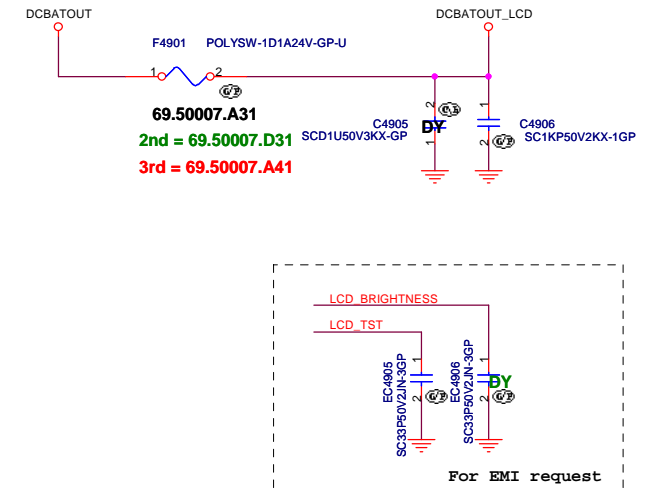
<Variant Name>

SSID = VIDEO



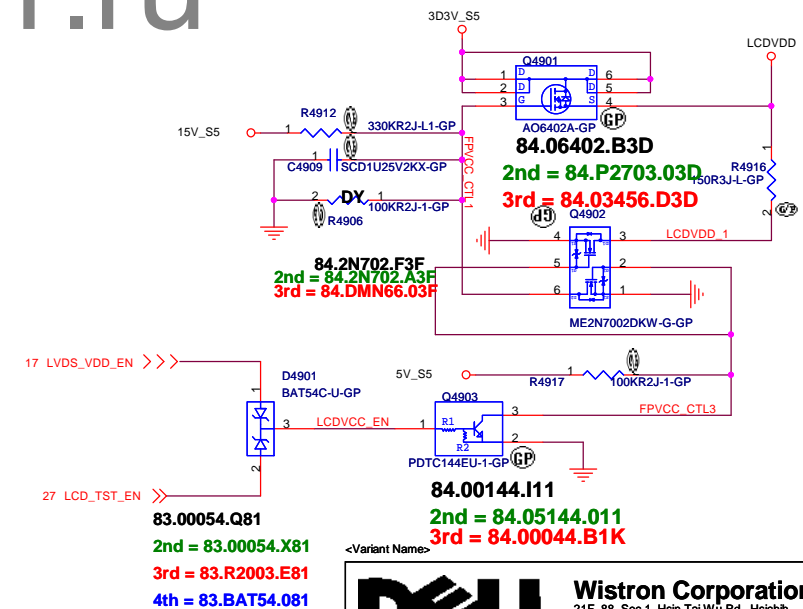
SSID = Inverter

INVERTER POWER

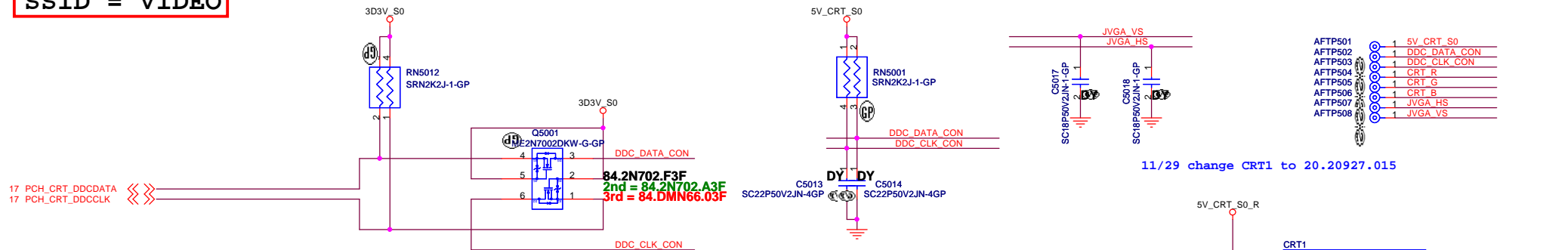


SSID = VIDEO

LCD POWER

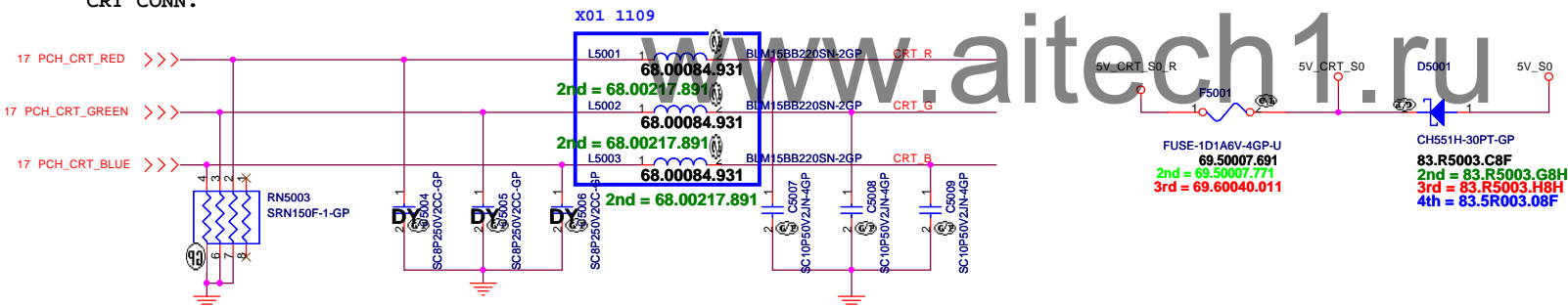


SSID = VIDEO

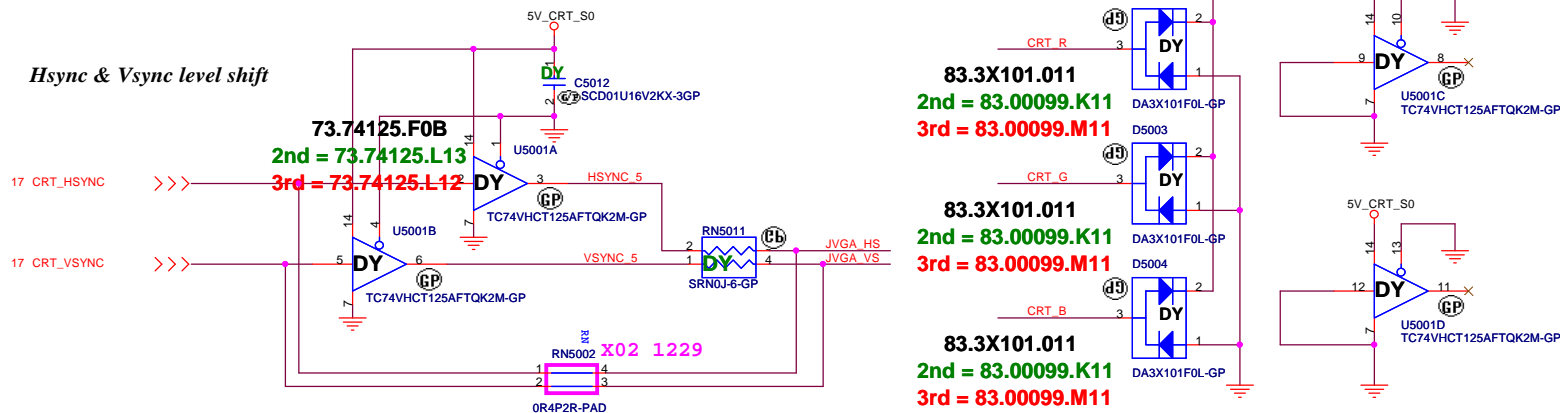


Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



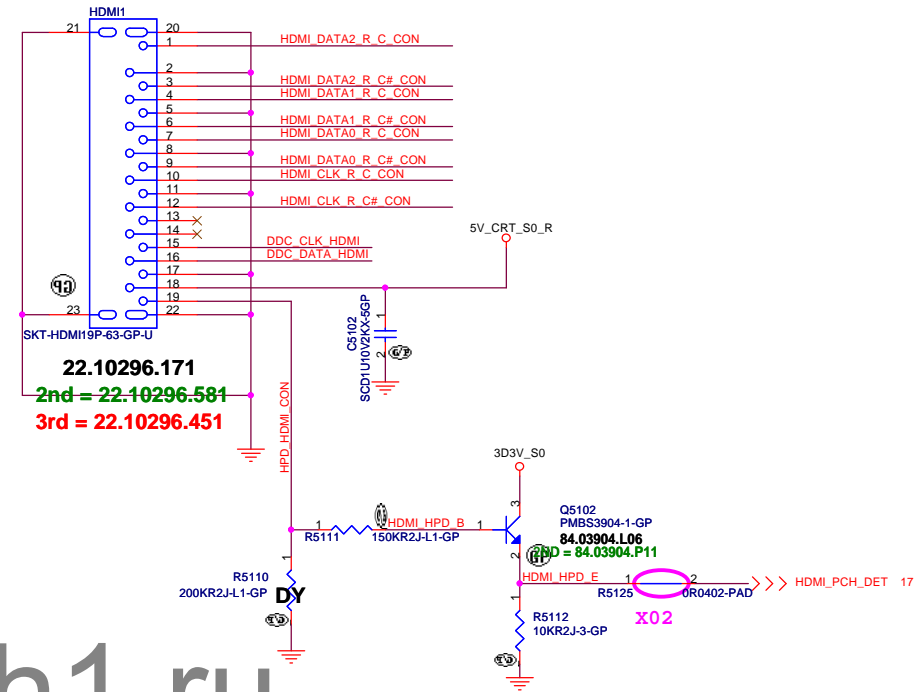
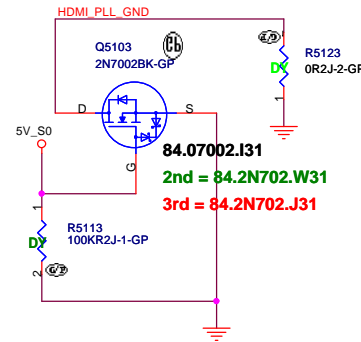
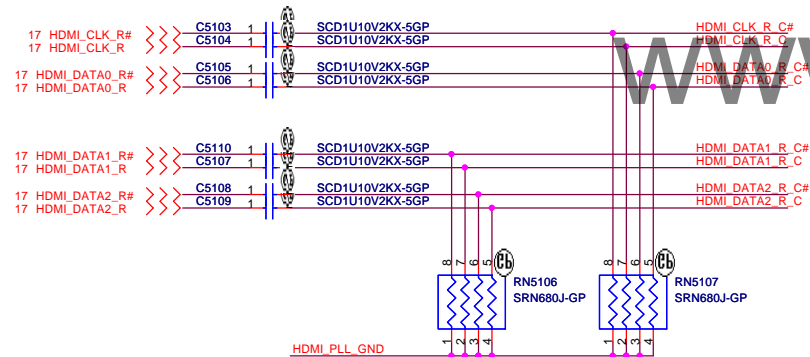
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

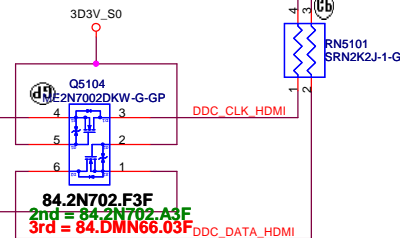
HDMI CONN

X02 1229

HDMI_CLK_R_C 1 R5101 2 HDMI_CLK_R_C.CON 0R0402-PAD
HDMI_DATA1_R_C 1 R5106 2 HDMI_DATA1_R_C.CON 0R0402-PAD
HDMI_CLK_R_C# 1 R5102 2 HDMI_CLK_R_C#.CON 0R0402-PAD
HDMI_DATA1_R_C# 1 R5105 2 HDMI_DATA1_R_C#.CON 0R0402-PAD
changed R5101,R5102 to short pad,
removed TR5101 CMC footprint
HDMI_DATA0_R_C 1 R5104 2 HDMI_DATA0_R_C.CON 0R0402-PAD
HDMI_DATA2_R_C 1 R5108 2 HDMI_DATA2_R_C.CON 0R0402-PAD
HDMI_DATA0_R_C# 1 R5103 2 HDMI_DATA0_R_C#.CON 0R0402-PAD
HDMI_DATA2_R_C# 1 R5107 2 HDMI_DATA2_R_C#.CON 0R0402-PAD
changed R5103,R5104 to short pad,
removed TR5103 CMC footprint
changed R5107,R5108 to short pad,
removed TR5104 CMC footprint



17_PCH_HDMI_CLK
17_PCH_HDMI_DATA



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Variant Name>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shifter/Connector			
Size: A3	Document Number: Enrico Caruso 14 MLK DIS	Rev: X02	
Date: Tuesday, January 03, 2012	Sheet: 51	of 104	

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<Variant Name>



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Title

Reserved

Size
A3

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X02


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<Variant Name>



Wistron Corporation
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Title

LVDS Switch

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A3

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<Variant Name>



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Title

Reserved

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SSID = User.Interface

(Blanking)

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<Variant Name>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

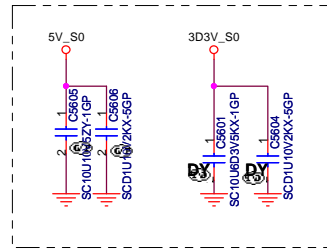
Title

ITP/Fan Connector

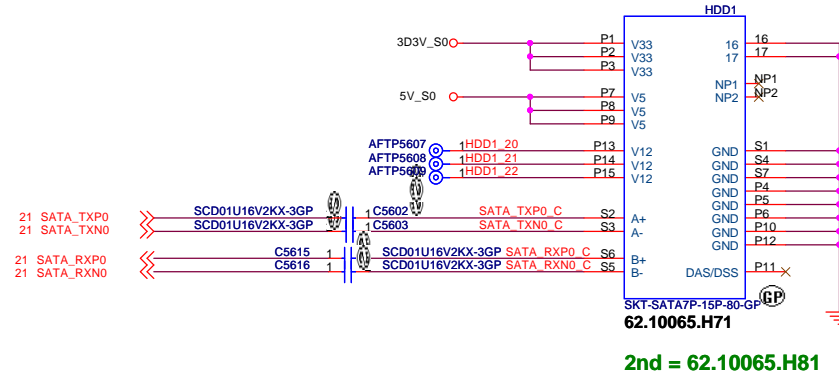
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
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SSID = SATA

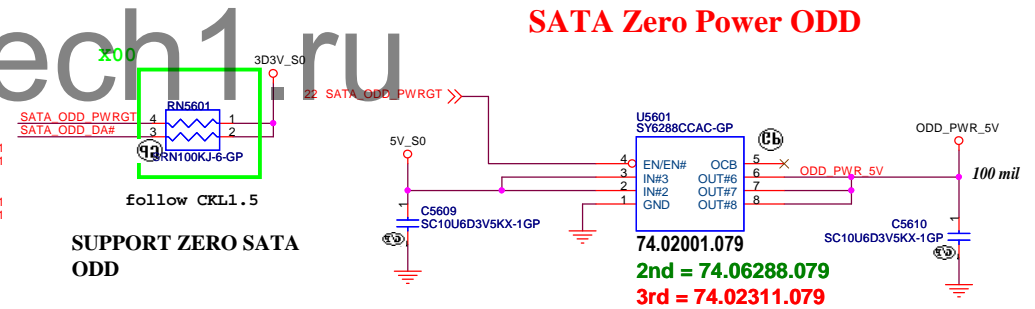
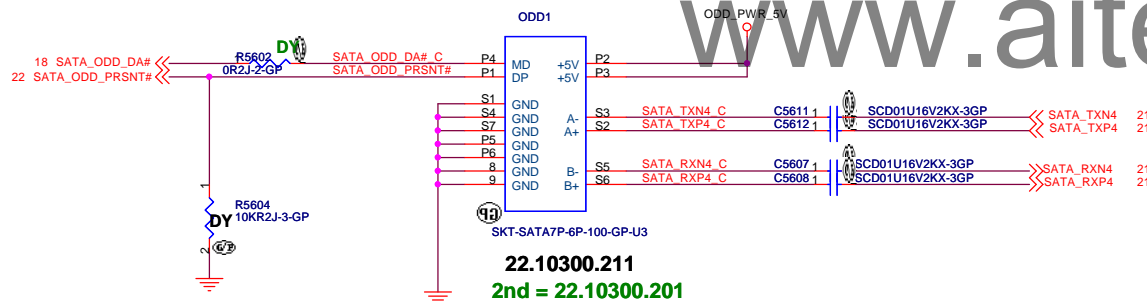
SATA HDD Connector



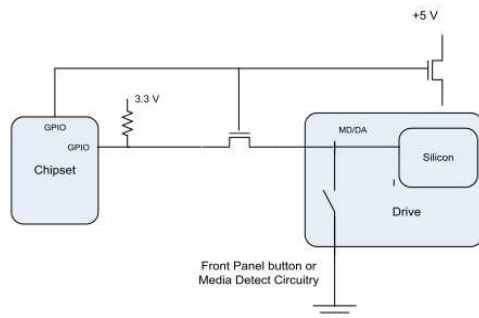
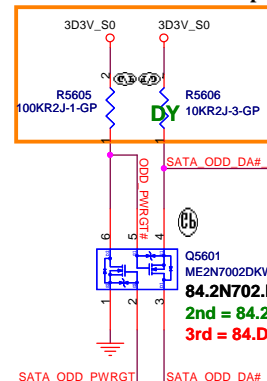
Close to HDD1



ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



<Variant Name>

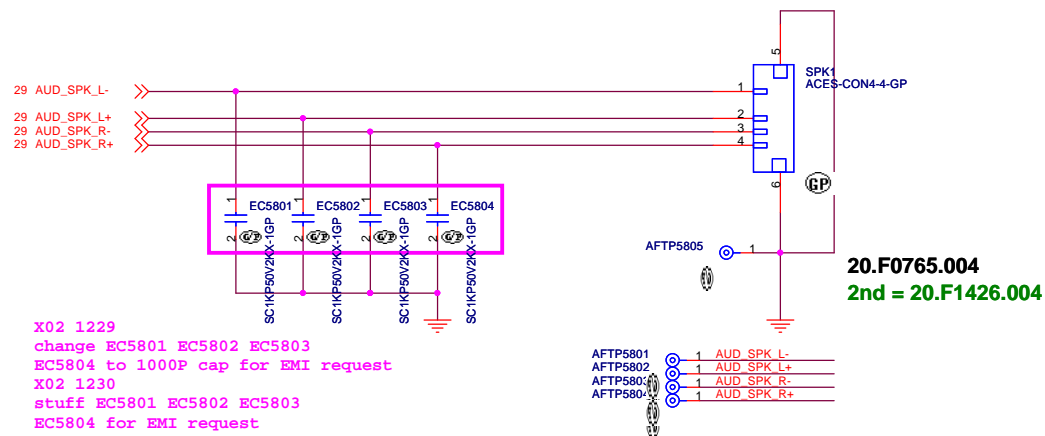
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = ESATA

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(Blanking)

SSID = AUDIO

Speaker Connector



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<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

SPEAKER CONN

Size
A3

Document Number

Enrico Caruso 14 MLK DIS

Rev

X02

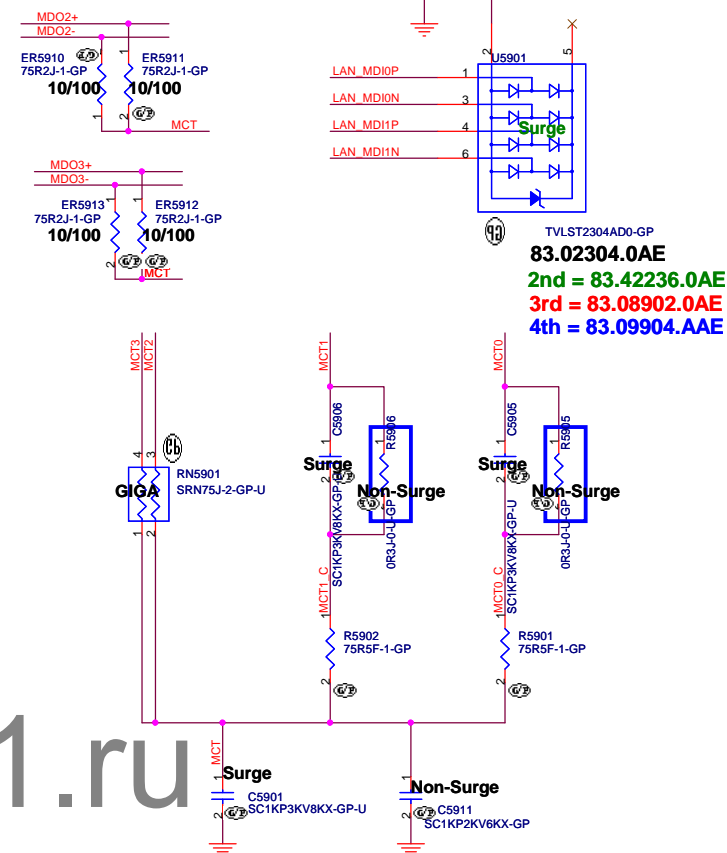
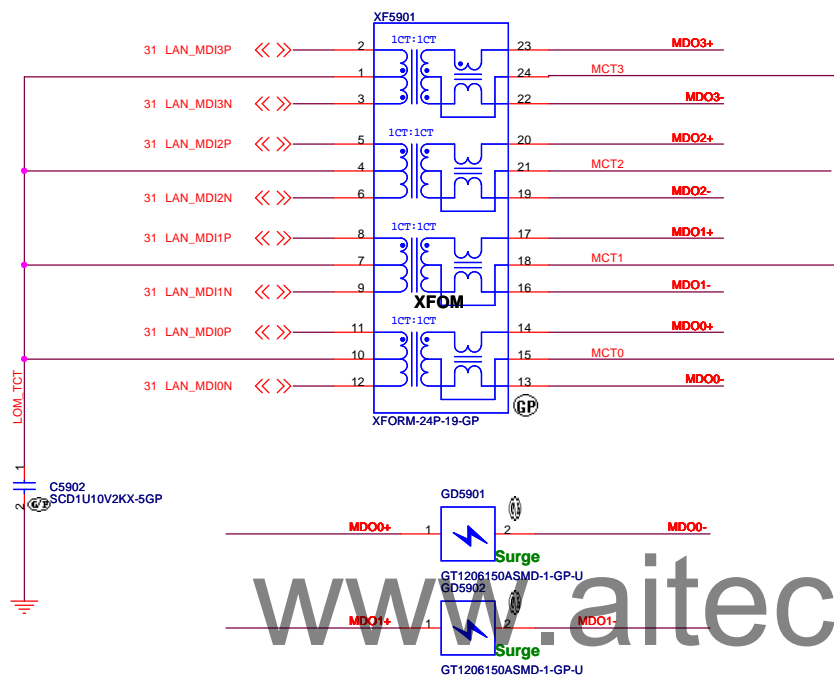
Date: Tuesday, January 03, 2012

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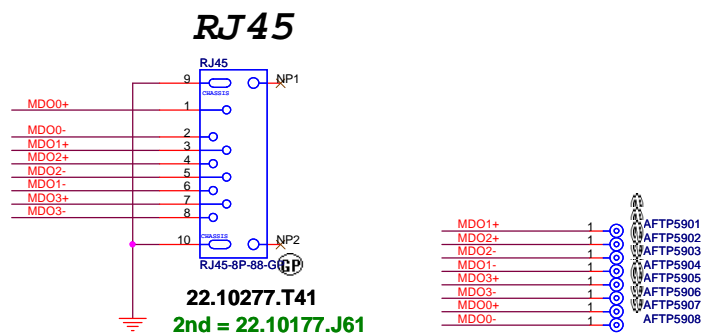
SSID = LOM

LAN TransFormer

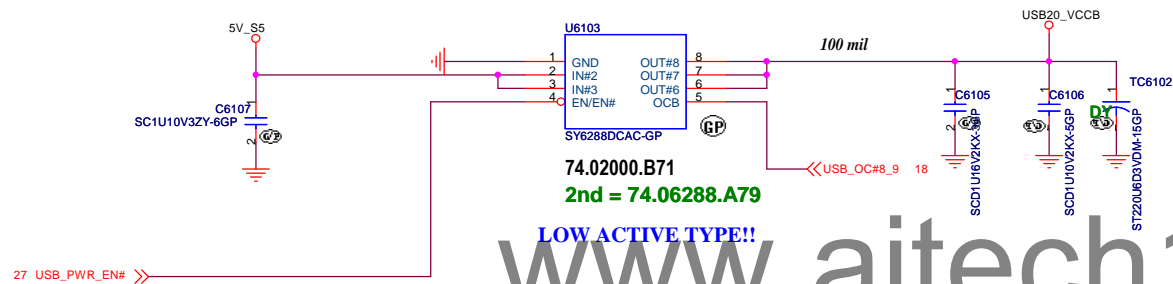
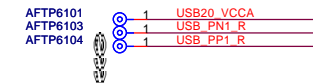
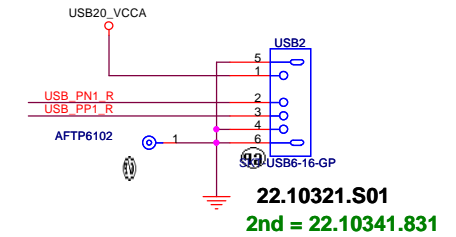
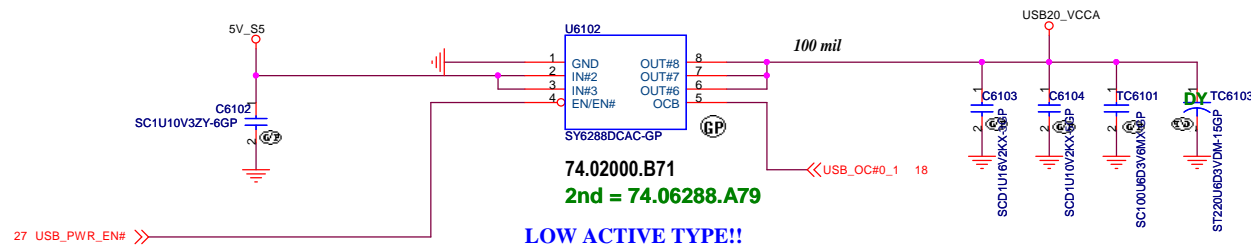
Giga Main: 68.IH106.30C
Giga 2ND: 68.05009.30A
10/100 Main: 68.HH085.301



0722 : change to gas tube



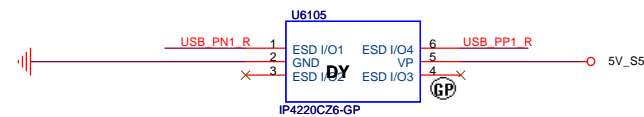
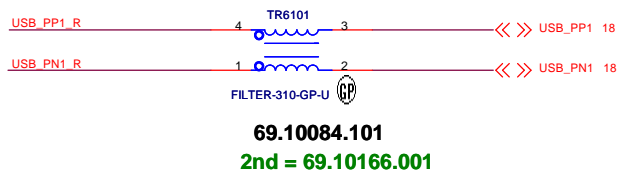
SSID = USB



LOW ACTIVE TYPE!!

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X02 1230
removed R6102,R6103 co-lay position



<Variant Name>



Wistron Corporation
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	Title
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USB Power SW

Size

Document Number

Rev	
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<Variant Name>



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Title

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SSID = User.Interface

(Blanking)

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<Variant Name>



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Title

Bluetooth

Size
A3

Document Number

Enrico Caruso 14 MLK DIS

Rev

X02

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(Blanking)

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<Variant Name>



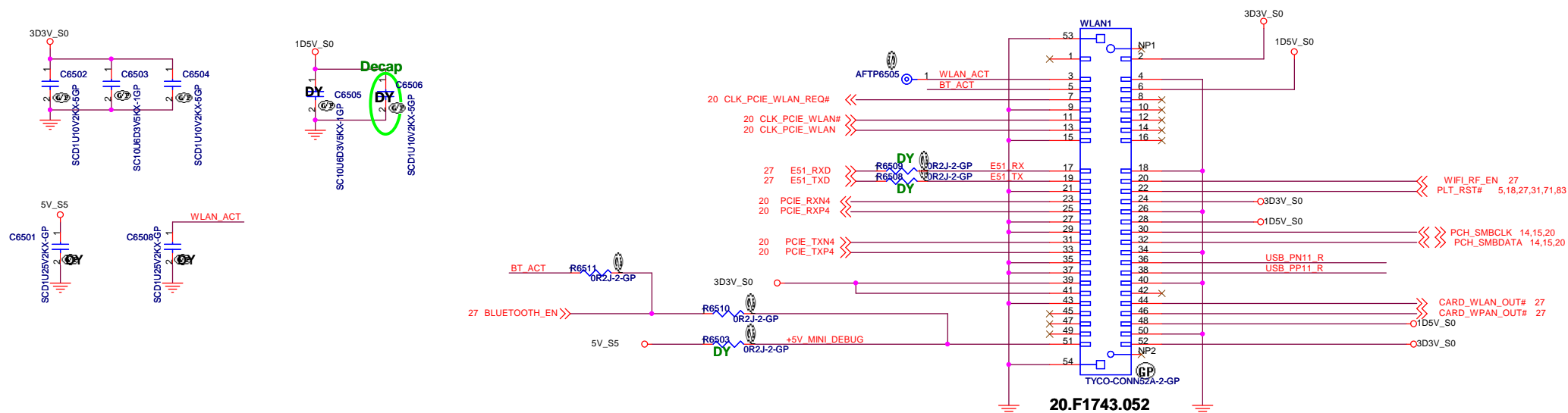
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A3	Enrico Caruso 14 MLK DIS	X02
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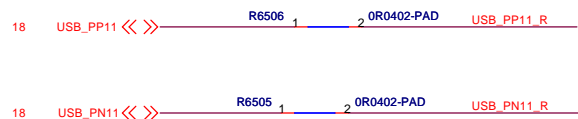
Mini Card Connector(802.11a/b/g)



20.F1743.052
2nd = 62.10043.A51
3rd = 62.10043.H01

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X02 1229
changed R6505,R6506 to short pad,
removed TR6501 CMC footprint



(Blanking)

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<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

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<Variant Name>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

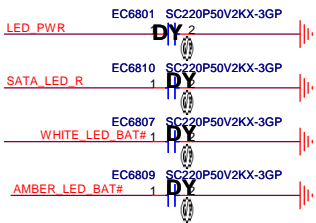
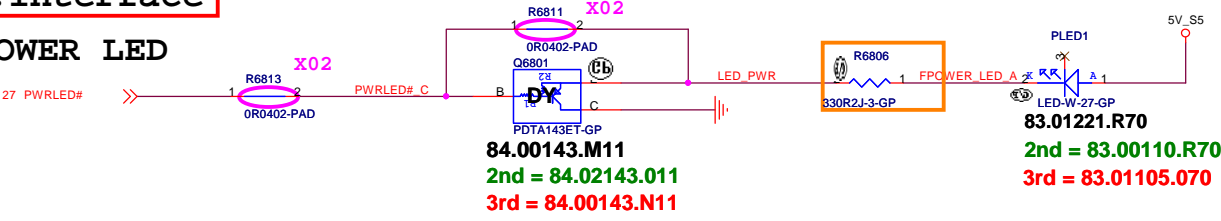
Size
A3

Document Number
Enrico Caruso 14 MLK DIS

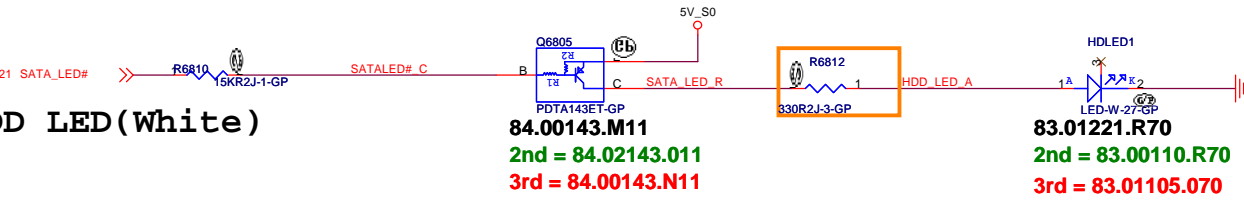
Rev
X02

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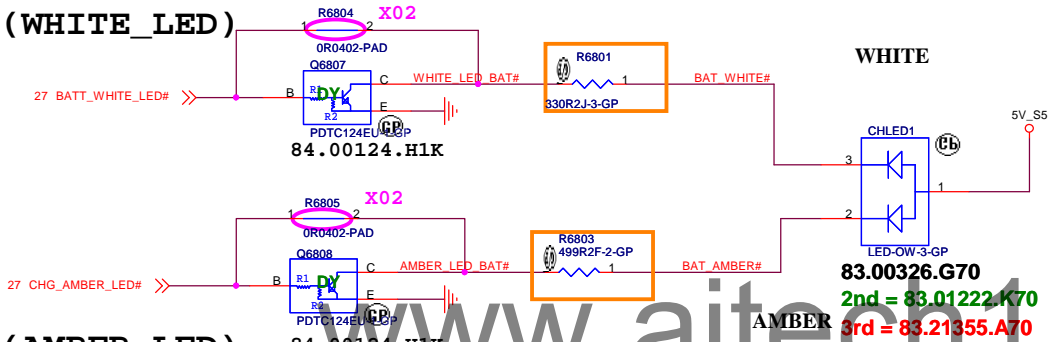
FRONT POWER LED



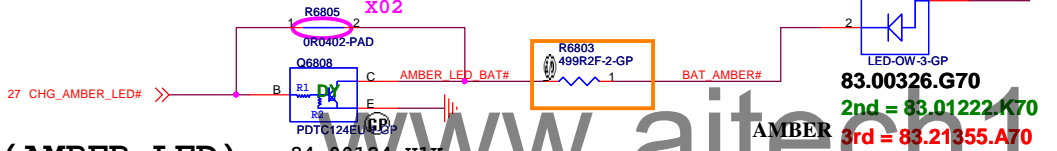
SATA HDD LED(White)



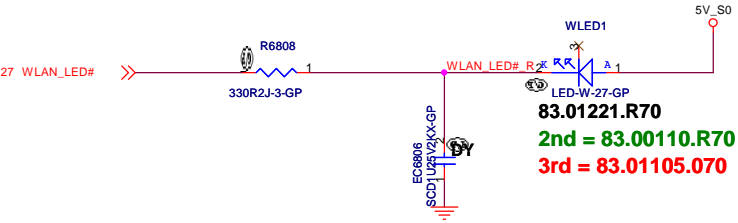
Battery LED2(WHITE_LED)



Battery LED1(AMBER_LED)

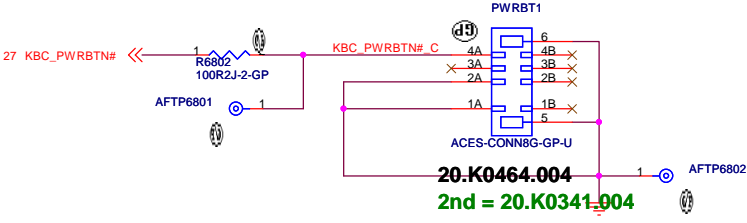


Wireless LED

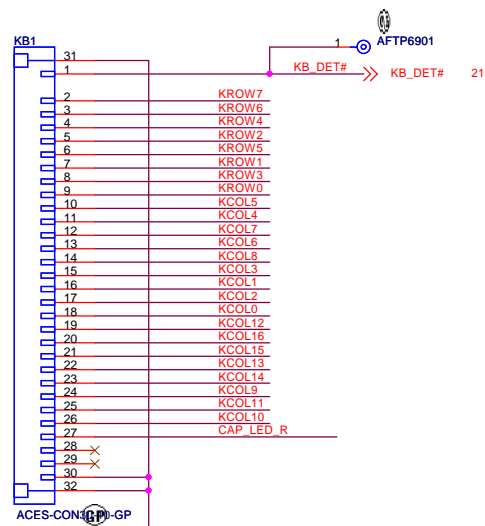


Place EC6806 near LED2

Power button



SSID = KBC



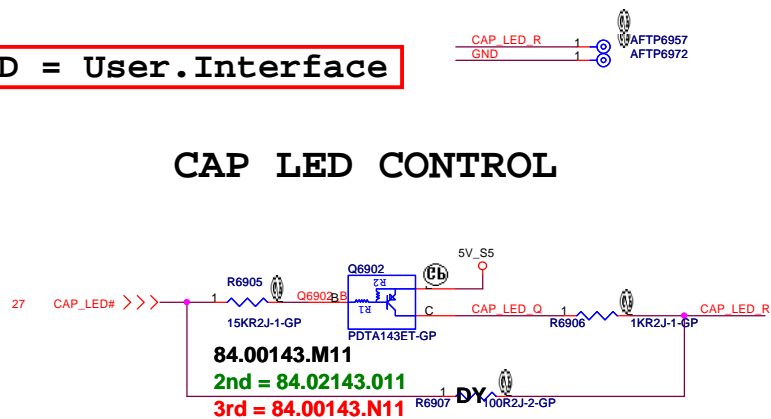
20.K0592.030

2nd = 20.K0621.030

3rd = 20.K0565.030

SSID = User.Interface

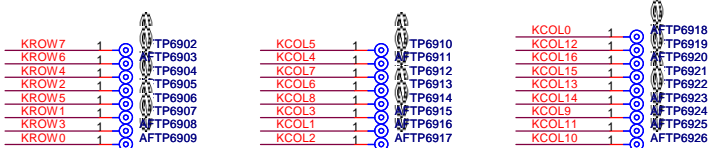
CAP LED CONTROL



84.00143.M11

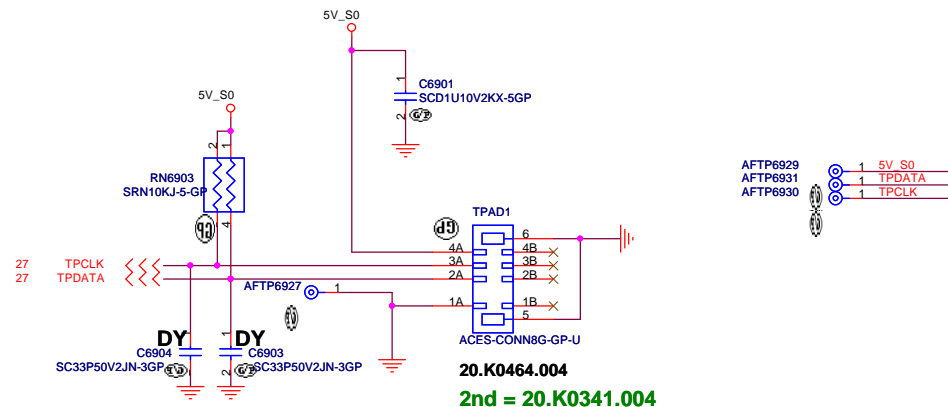
2nd = 84.02143.011

3rd = 84.00143.N11



SSID = Touch.Pad

TouchPad Connector



20.K0464.004

2nd = 20.K0341.004

<Variant Name>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size
A3

Document Number

Enrico Caruso 14 MLK DIS

Rev
X02

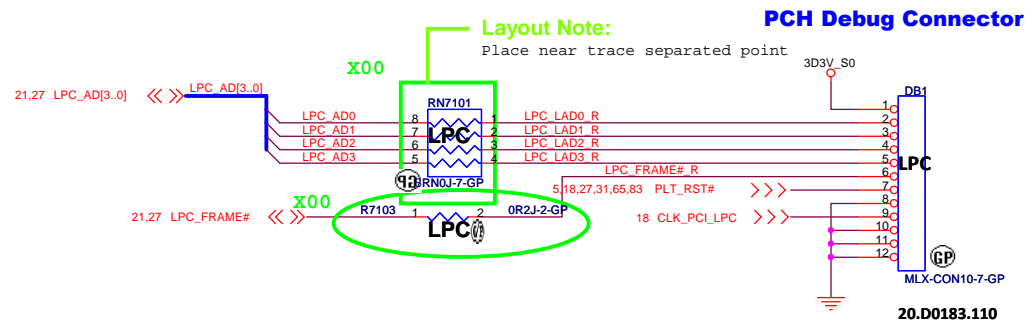
Date: Tuesday, January 03, 2012

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
Size A3	Document Number Enrico Caruso 14 MLK DIS		Rev X02
Date: Friday, December 30, 2011	Sheet 70 of 104		



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<Variant Name>



Title			Debug connector	
Size A3	Document Number		Rev X02	
Date: Tuesday, January 03, 2012	Sheet 71 of 104		Enrico Caruso 14 MLK DIS	

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<Variant Name>



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Title

Size
A3

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Enrico Caruso 14 MLK DIS

Date: Friday, December 30, 2011

Reserved

Rev
X02

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Title

Reserved

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3D3V_CARD_S0

3.3V

5V

D7401

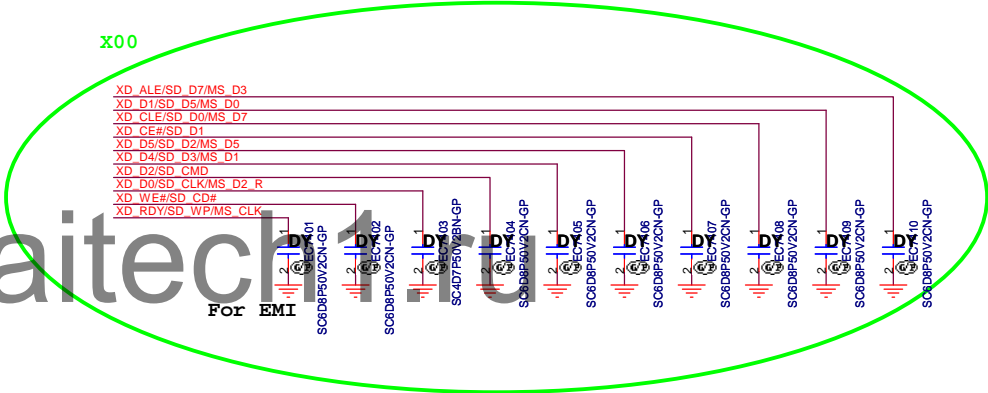
D7402

C7403

C7404

SC2D24UBD3V3KX-5GP

SC2D24UBD5V3KX-5GP



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SSID = ExpressCard

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Title

Express Card

Size
A3

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<Variant Name>



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Title

Reserved

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Title

Reserved

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Title

Reserved

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SSID = User.Interface

(Blanking)
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(Blanking)

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Title

Reserved

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(Blanking)

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<Variant Name>



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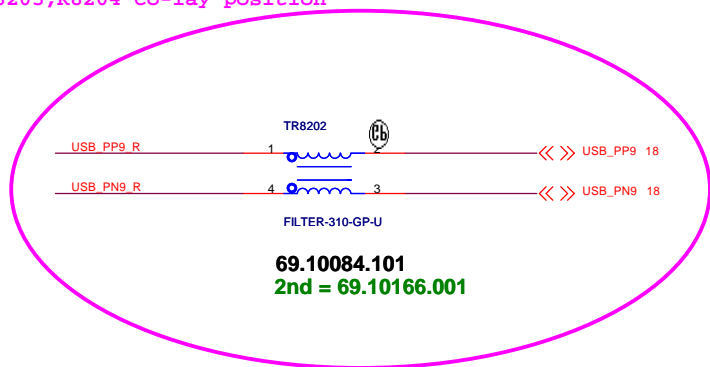
Title

Reserved

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 81 of	104

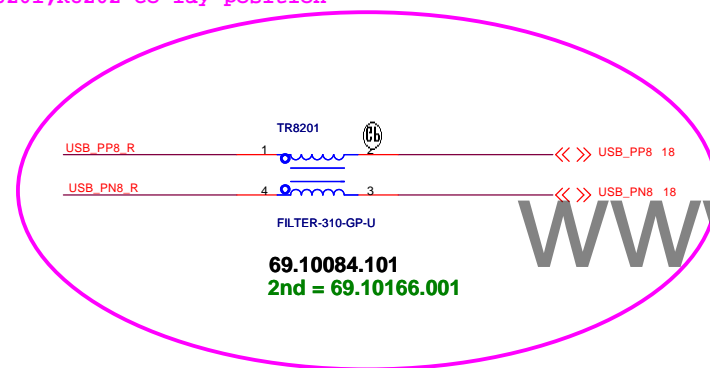
SSID = USB

X02 1230
removed R8203,R8204 co-lay position



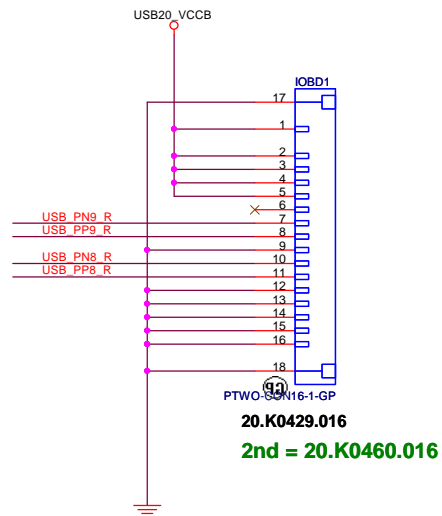
69.10084.101
2nd = 69.10166.001

X02 1230
removed R8201,R8202 co-lay position



69.10084.101
2nd = 69.10166.001

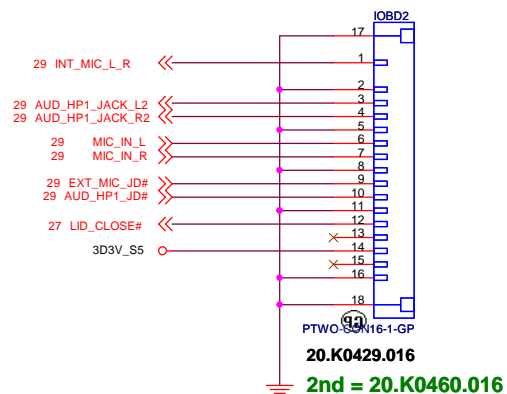
IOBD1 is for USB board



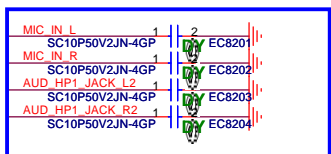
20.K0429.016
2nd = 20.K0460.016

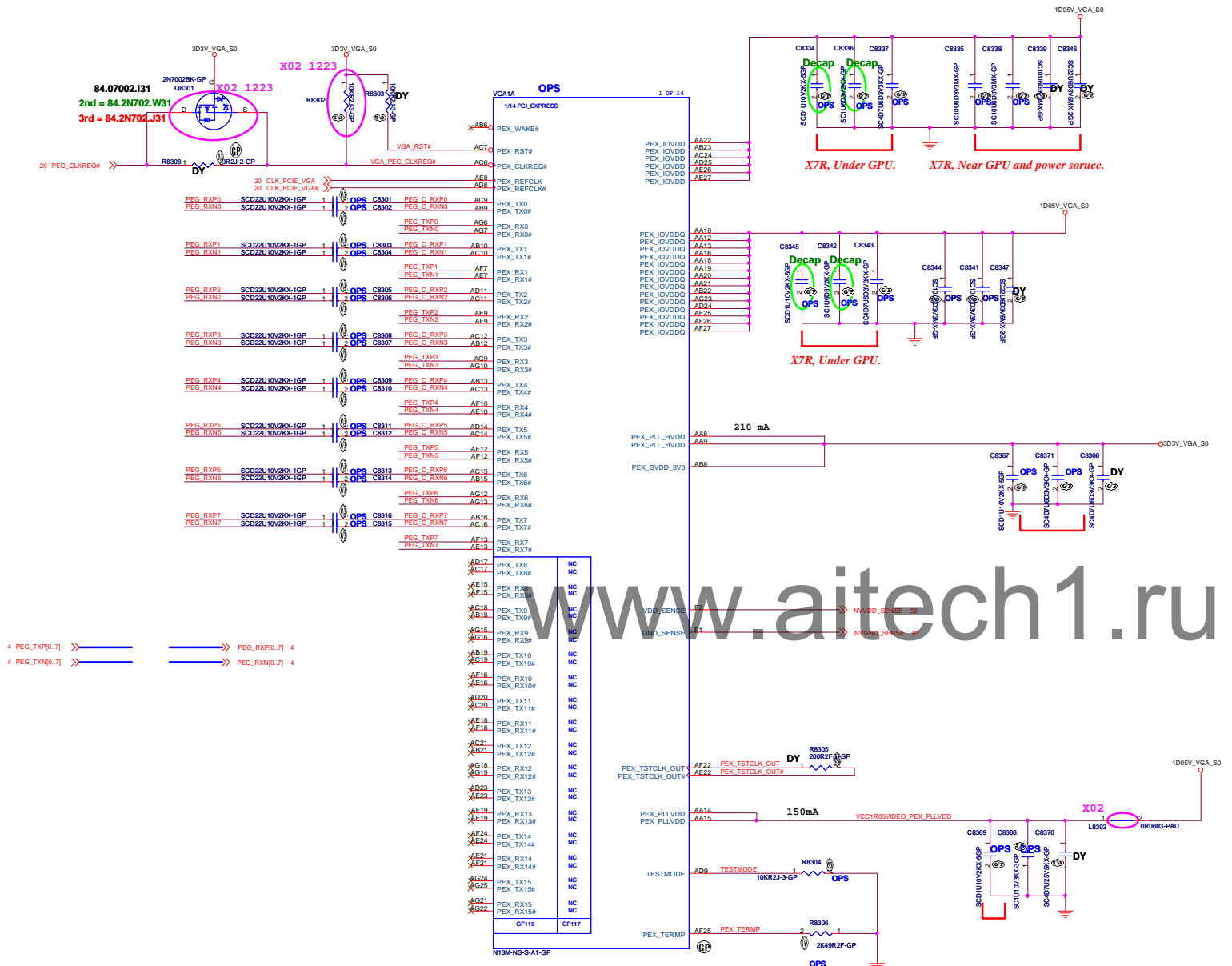
SSID = Audio

IOBD2 is for Audio board

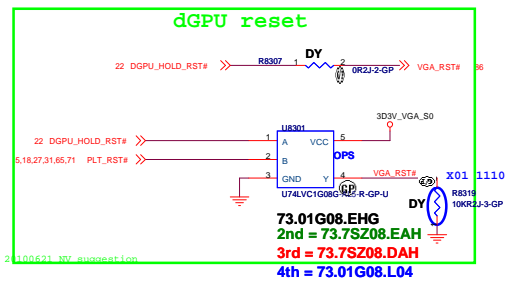


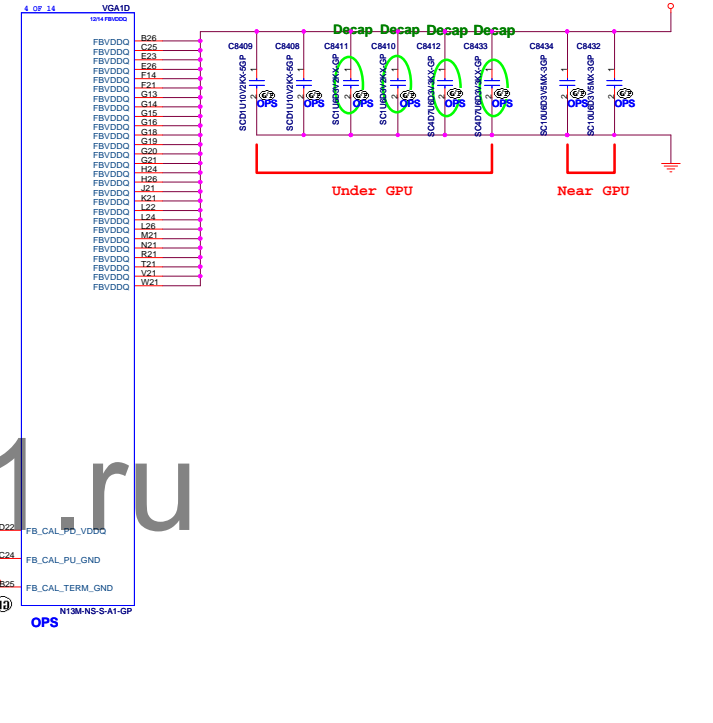
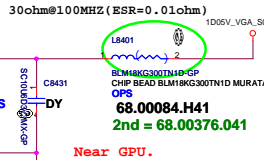
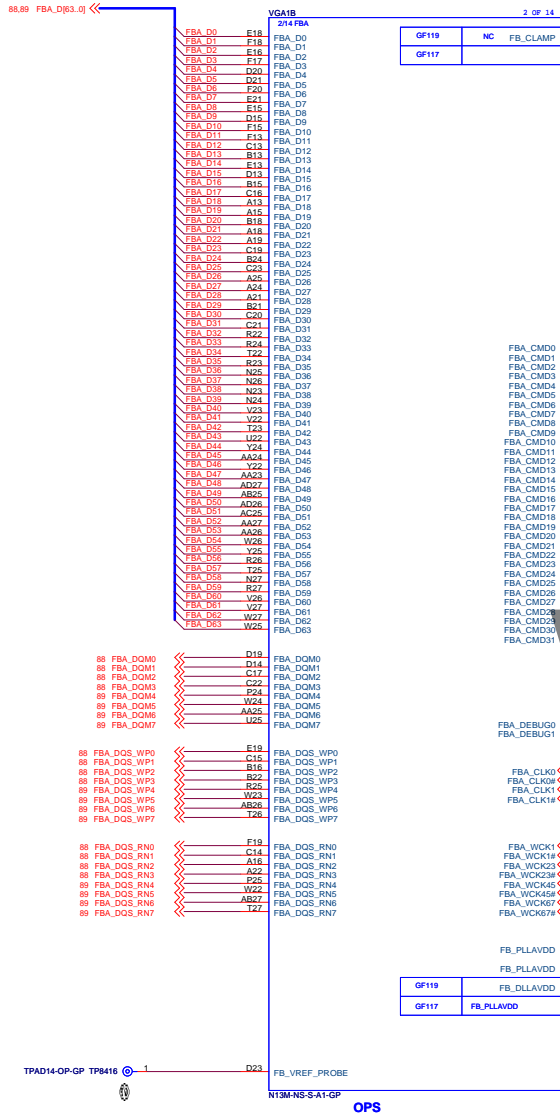
20.K0429.016
2nd = 20.K0460.016





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VGA1G 7. GP 34

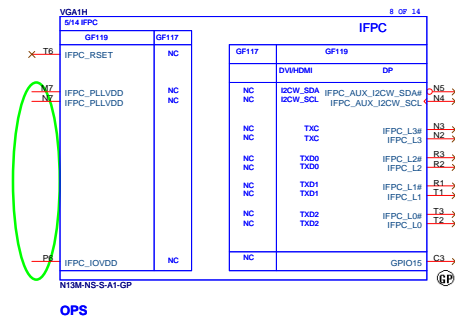
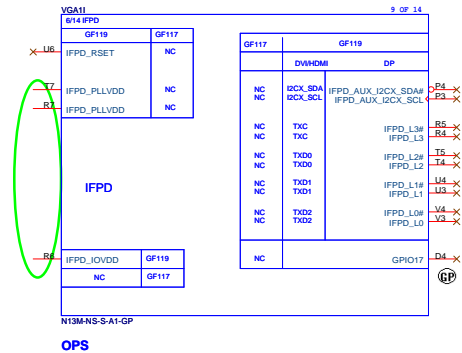
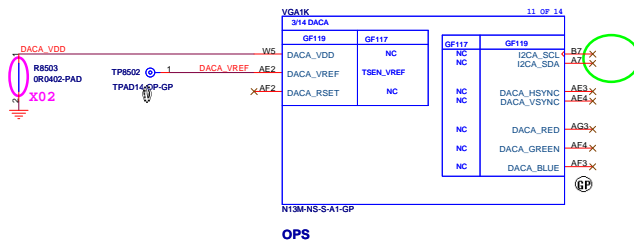
4/14 (FPA8)

GF119		GF117
IFPA_RSET	NC	IFPA_TXC8 IFPA_TXC1
IFPAB_PLLVDD	NC	IFPA_TXD08 IFPA_TXD0
IFPAB_PLLVDD	NC	IFPA_TXD1# IFPA_TXD1
		IFPA_TXD28 IFPA_TXD2
		IFPA_TXD3# IFPA_TXD3
		IFPB_TXC8 IFPB_TXC
IFPA_IOVDD	NC	IFPB_TXD4# IFPB_TXD4
IFPB_IOVDD	NC	IFPB_TXD5# IFPB_TXD5
		IFPB_TXD6# IFPB_TXD6
		IFPB_TXD7# IFPB_TXD7
		GPIO14

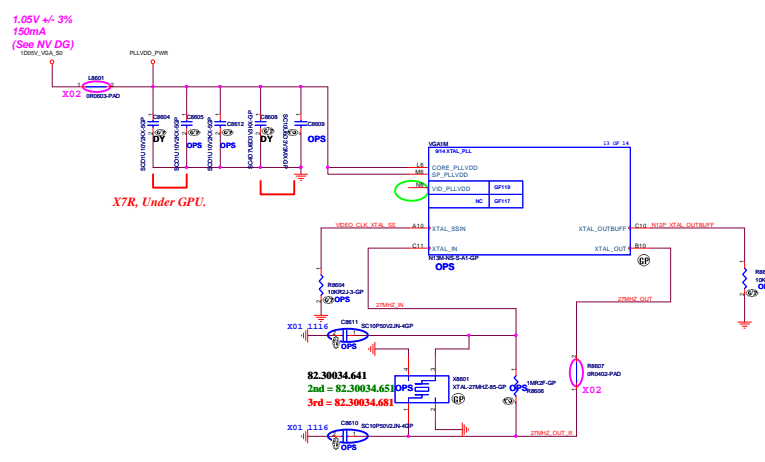
IFPAB

N13M-NS-A1-GP

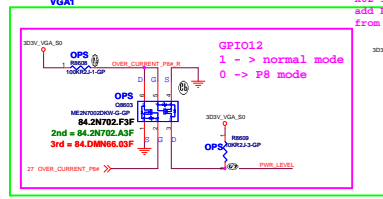
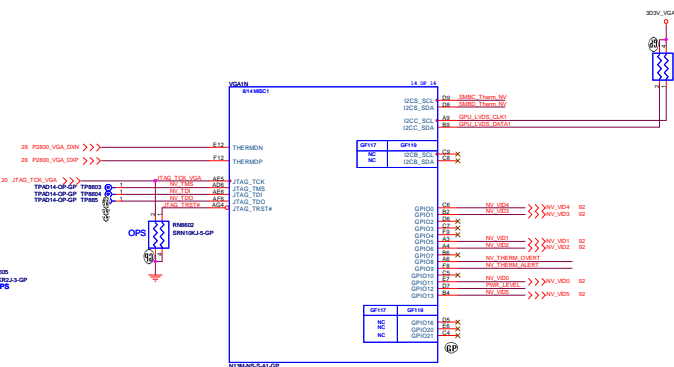
OP8



1.05V +/- 3%
150mA
(See NV DG)
100V, VGA, SD



I2CA=>CRT, I2CC=>LVDS.

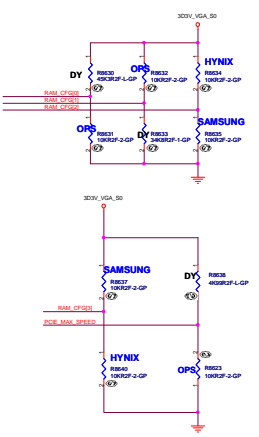
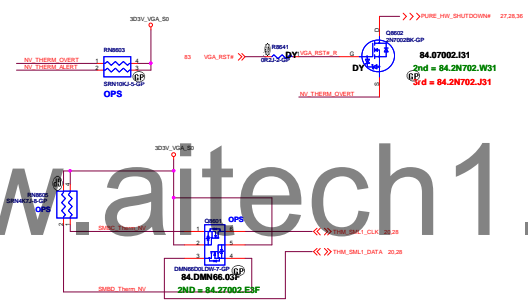


X02 1230
add R8608,Q8603;change Q8603.2 to OVER CURRENT_P8
from AC_PRESENT for OC trigger IPCC fuction

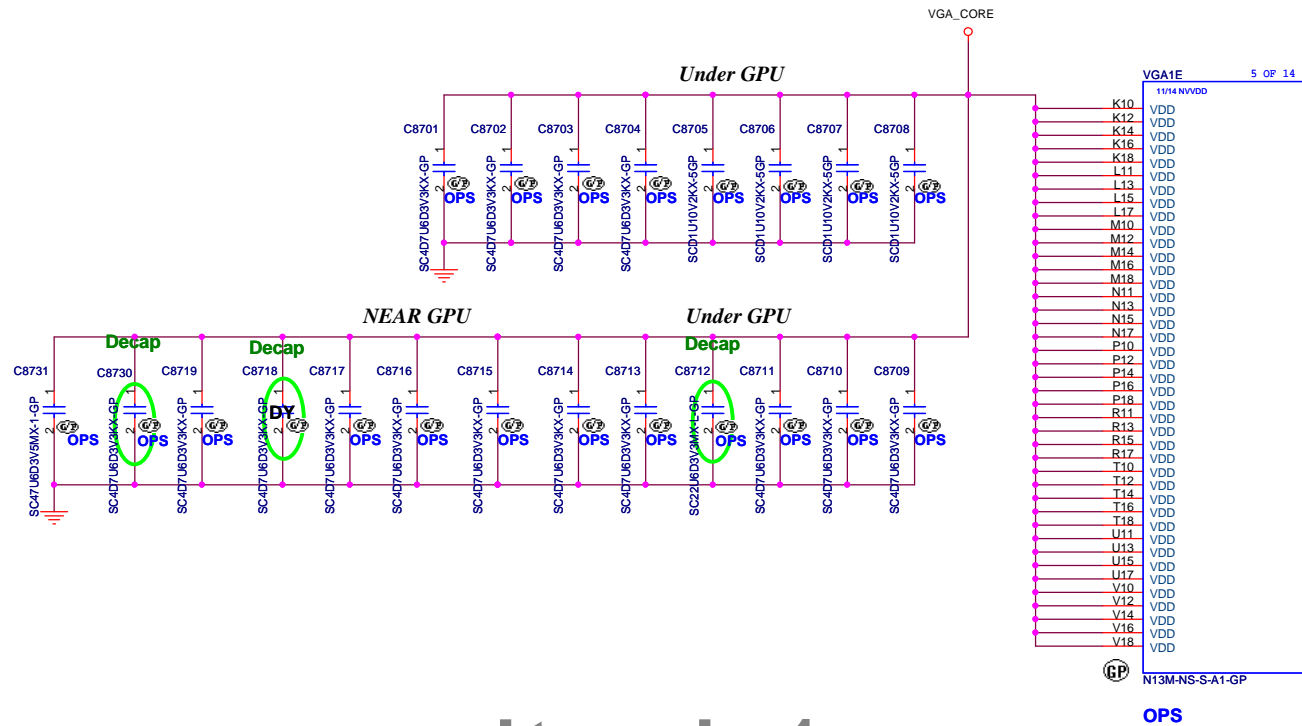
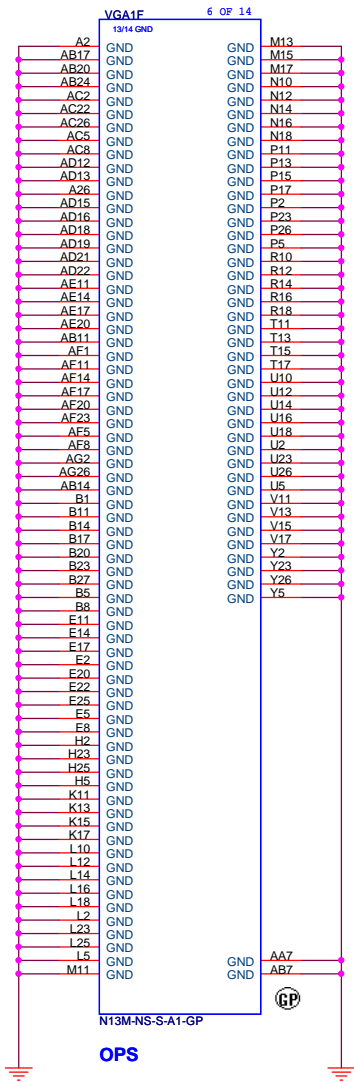
Hynix:72.52G63.A0U (HT31PSAA)
Samsung:72.42164.D0U (J1P0F2SAA)

Strap Pin Nmae	Strap mapping	Resistance	Polarity(Samsung@+)	Polarity(Hynix@+)
ROM_SCLK	SMB_ALT_ADDR	10K ohm	pull down to GND	pull down to GND
ROM_SI	SUB_VENDOR	10K ohm	pull down to GND if no VBIOS ROM	pull down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10K ohm	pull down to GND(no display)	pull down to GND(no display)
STRAP0	RAM_CFG0	10K ohm	pull down to GND	pull down to GND
STRAP1	RAM_CFG1	10K ohm	pull up to 3.3V	pull up to 3.3V
STRAP2	RAM_CFG2	10K ohm	pull down to GND	pull up to 3.3V
STRAP3	RAM_CFG3	10K ohm	pull up to 3.3V	pull down to GND
STRAP4	PCIE_MAX_SPEED	10K ohm	pull down to GND	pull down to GND

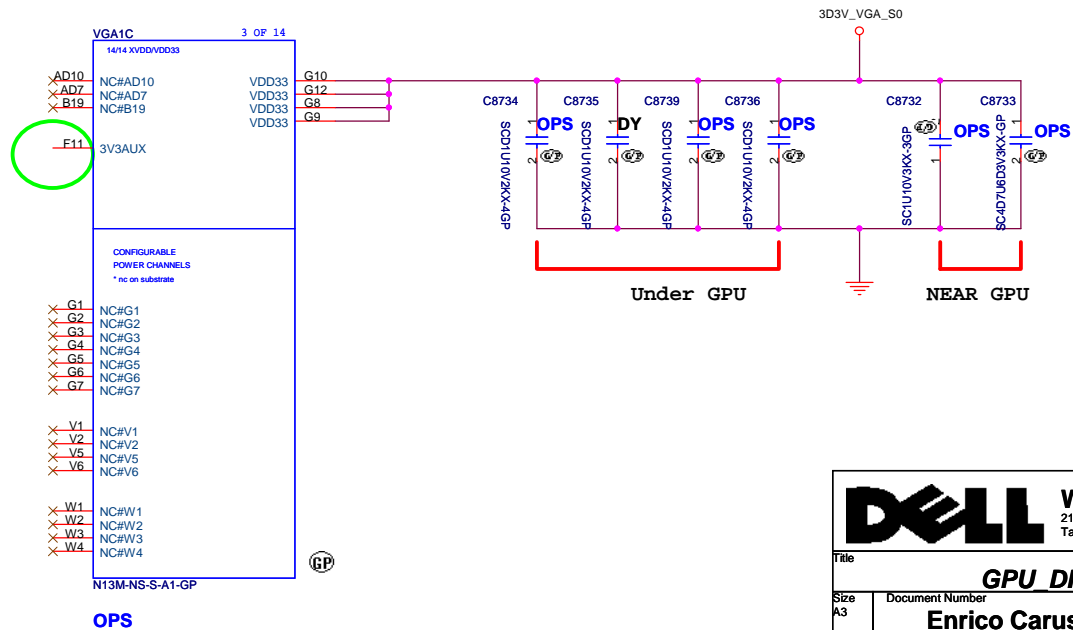
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N13x GPUs do not support CEC. Leave the CEC pin as NC



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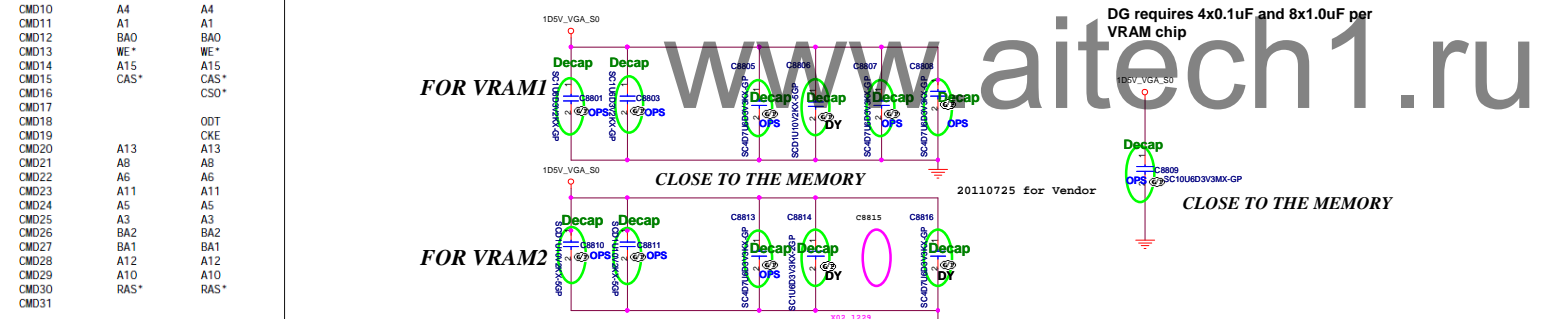
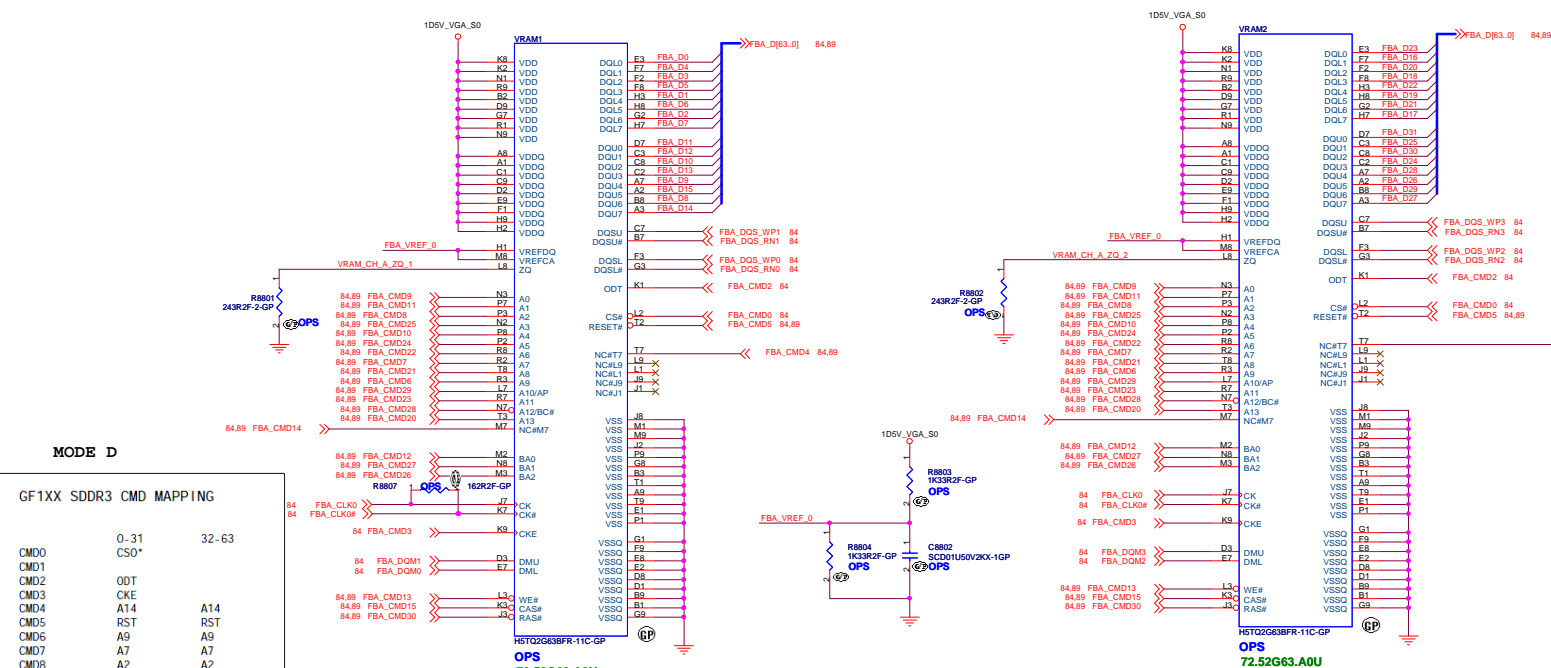


MODE D

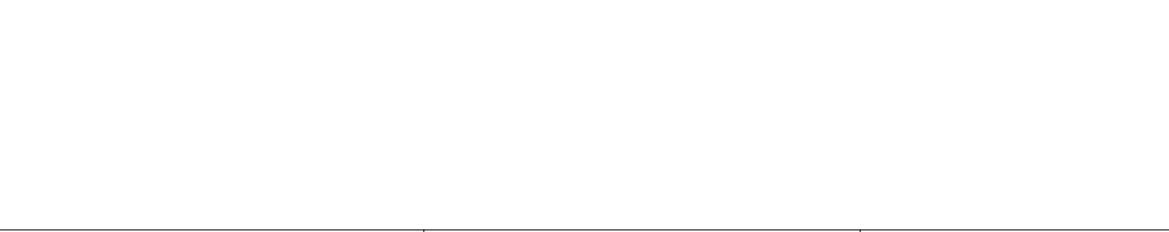
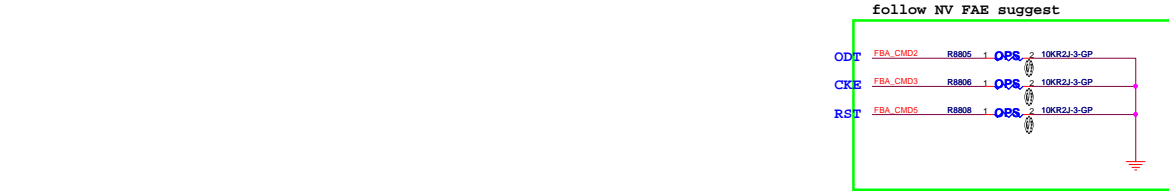
GF1XX SDDR3 CMD MAPPING

CMD0	0-31	32-63
CMD1	CS0*	
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16	CS0*	
CMD17		
CMD18	ODT	
CMD19	CKE	
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
CMD31		

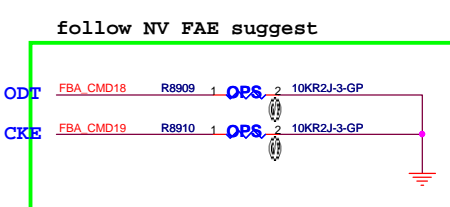
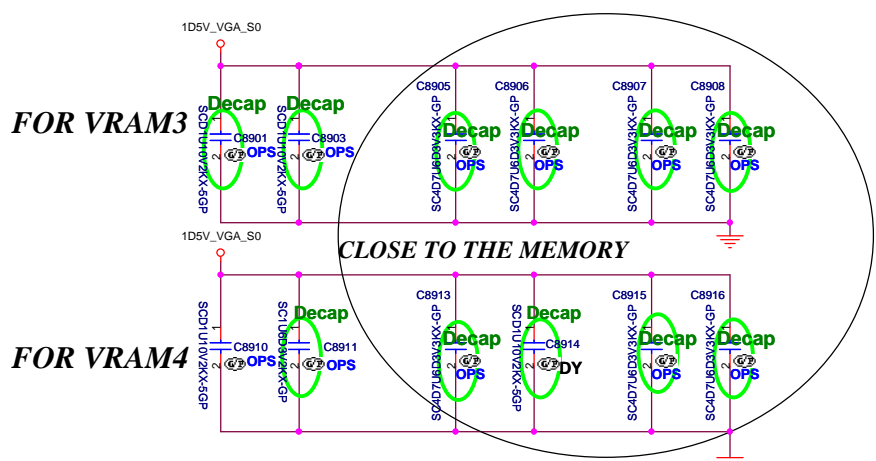
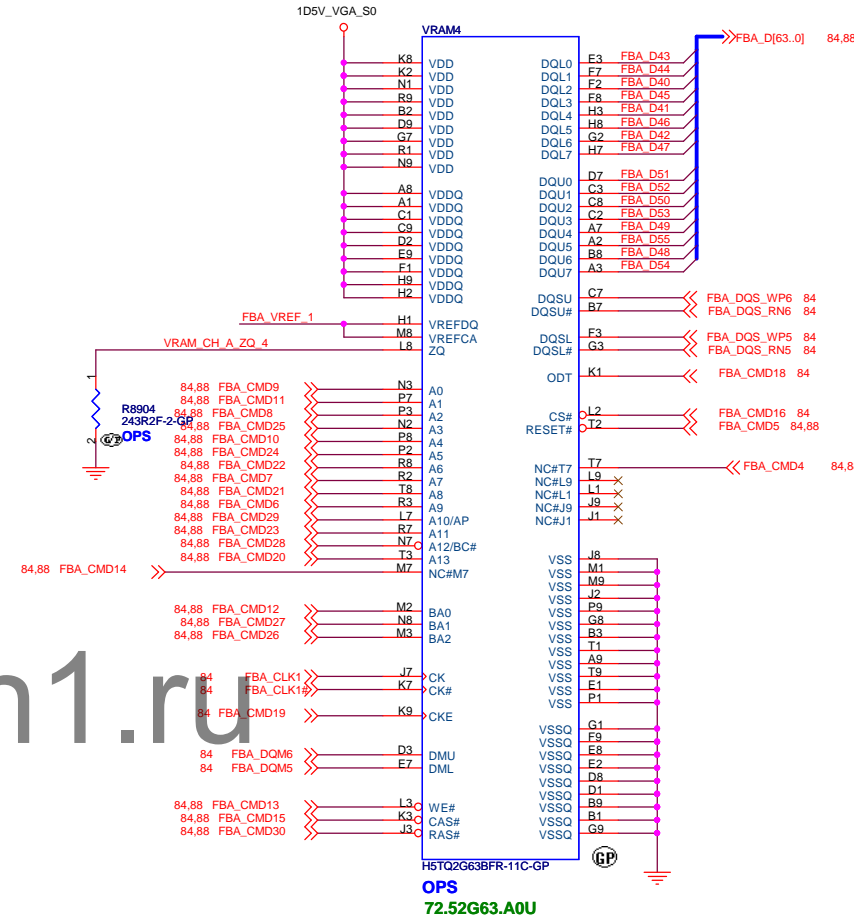
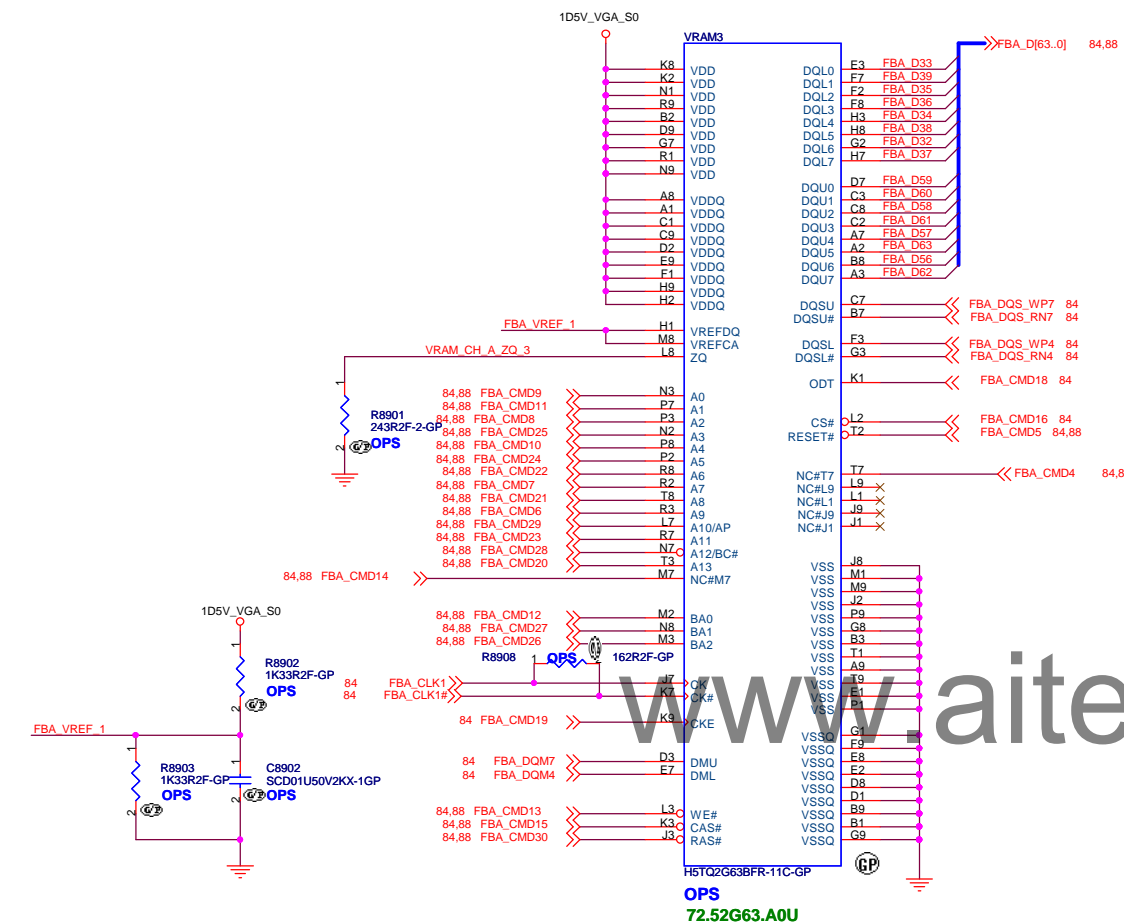
* A15 is not required for any x16 device, even up to 4Gb density
 * A15 is only needed if we support x8 configurations, and only at 4Gb



* A15 is not required for any x16 device, even up to 4Gb density
 * A15 is only needed if we support x8 configurations, and only at 4Gb



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CLOSE TO THE MEMORY

(Blanking)

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<Variant Name>



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Title


GPU-VRAM5,6 (3/4)

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
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(Blanking)

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<Variant Name>



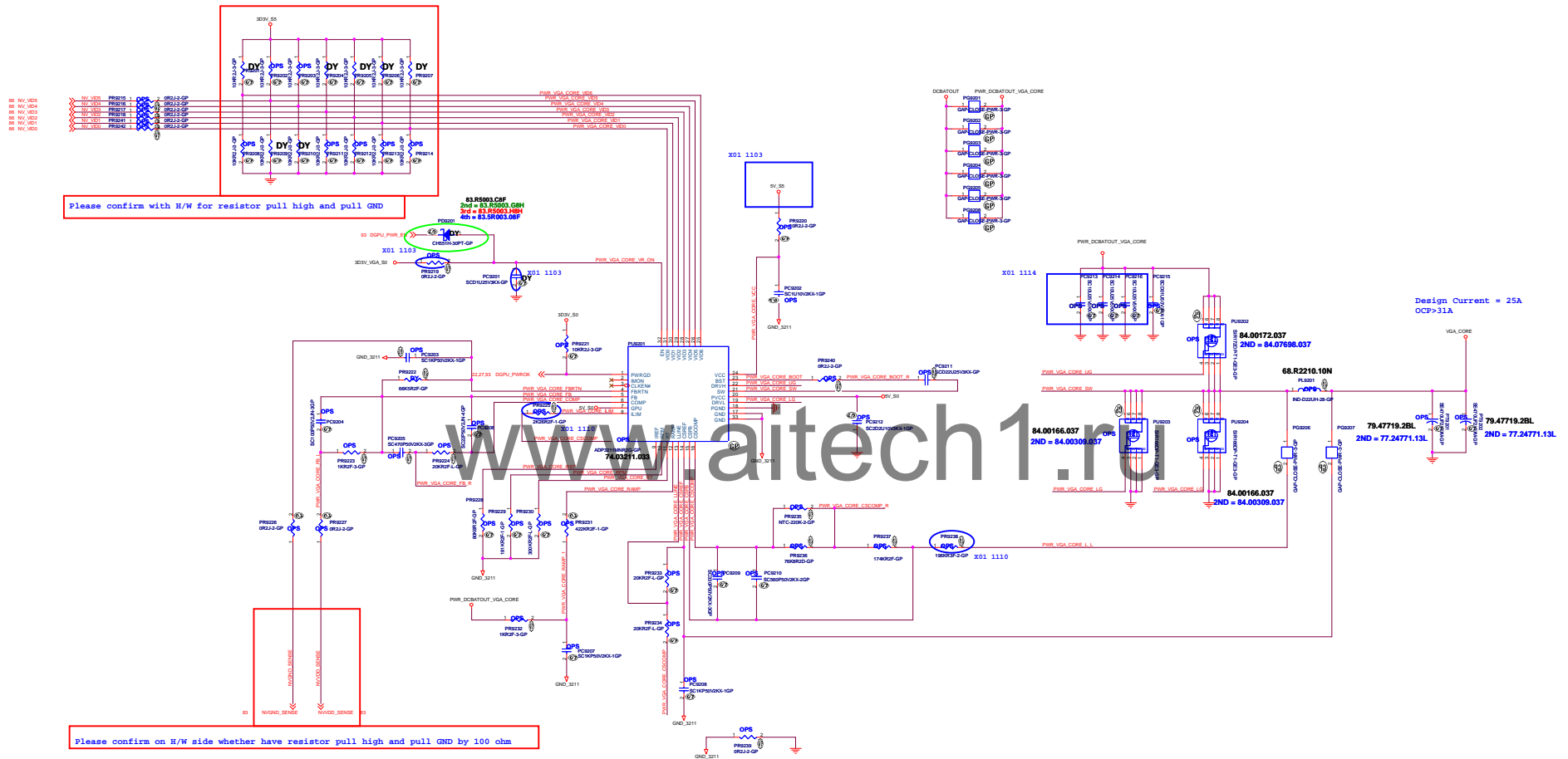
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Title

GPU-VRAM7,8 (4/4)


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V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0



(Blanking)
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<Variant Name>



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Title

LVDS Switch

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<Variant Name>



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Title

CRT Switch

Size
A3

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SSID = SDIO

(Blanking)
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<Variant Name>



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Title

TOUCH PANEL

Size
A3

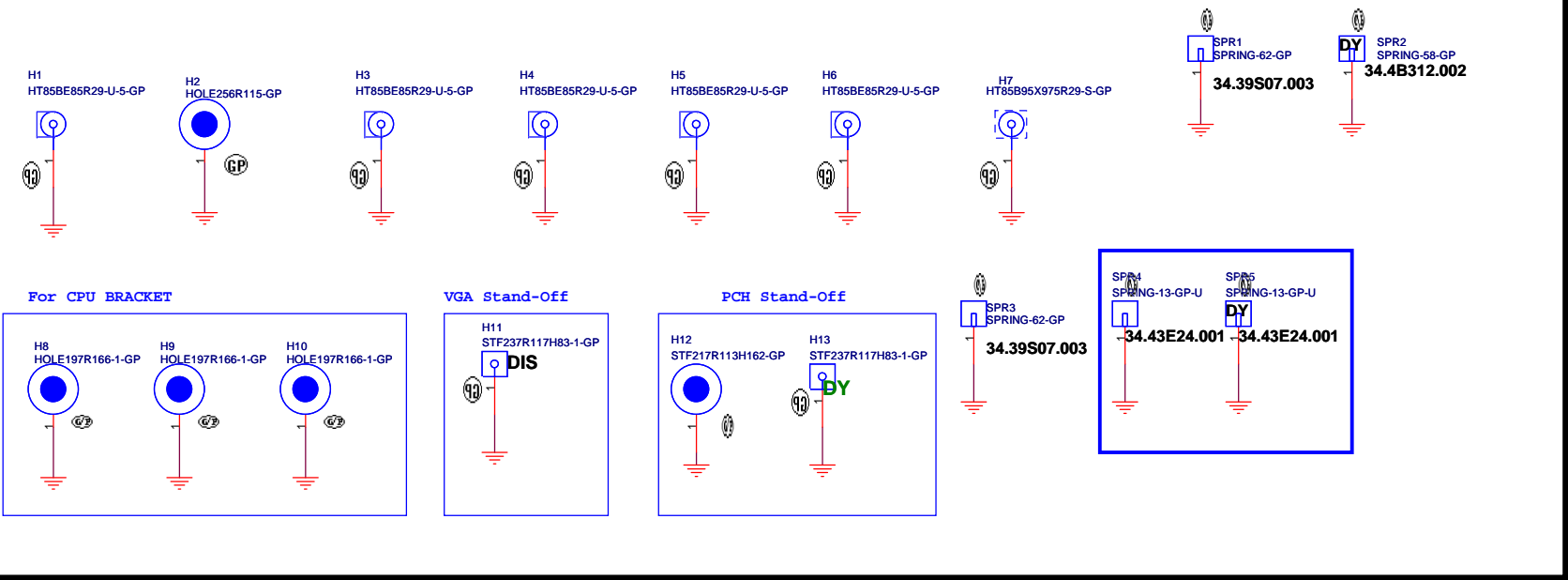
Document Number
Enrico Caruso 14 MLK DIS

Rev
X02

Date: Friday, December 30, 2011

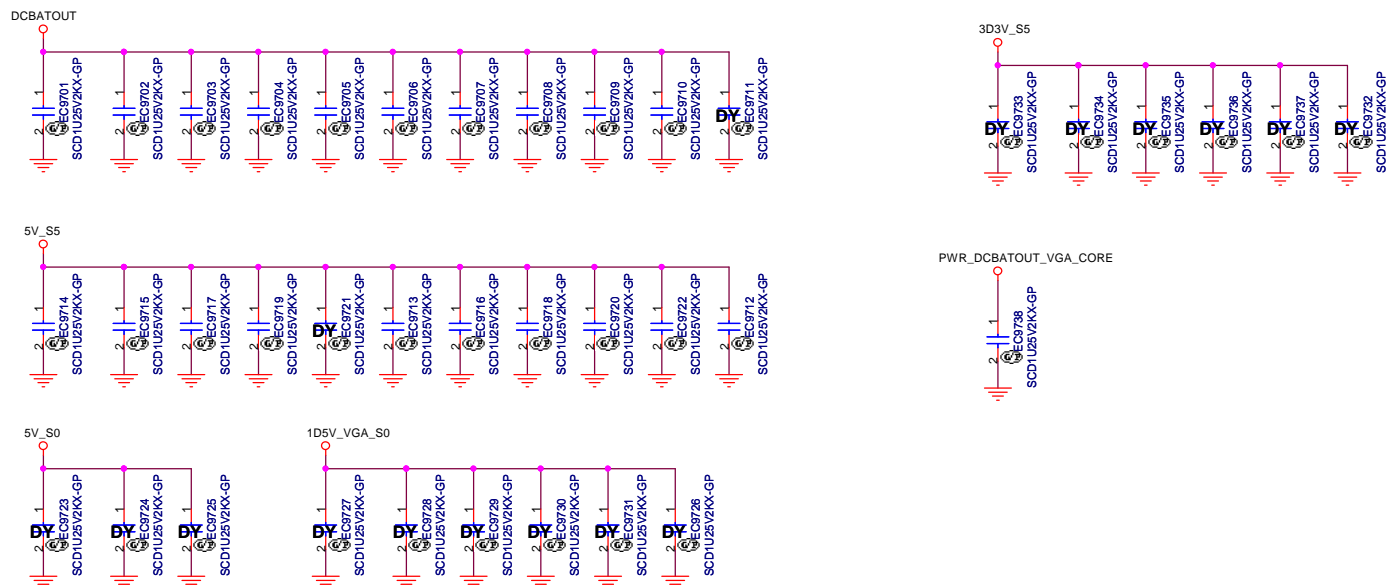
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SSID = Mechanical



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SSID = EMI



<Variant Name>

DELL

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Title

UNUSED PARTS/EMI Capacitors

Size

Document Number

Enrico Caruso 14 MLK DIS

Rev	
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A3

Enrico C

Enrico Caruso 14 MLK DIS

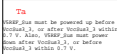
X02

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(AC mode)

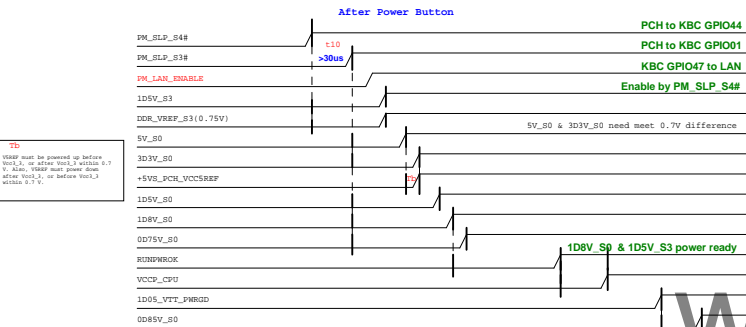
Within logic high level and disable
it is less than the logic low level.



Not floating.

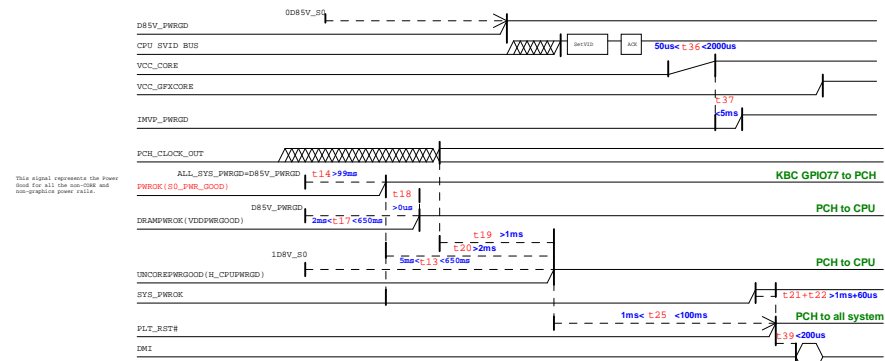
sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.



Tb

VREF must be powered up before Voc1_3, or after Voc1_3 within 0.7 V. Also, VREF must power down after Voc1_3, or before Voc1_3 within 0.7 V.



This signal represents the Power Good for all the non-CORE and non-graphics power rails.

The diagram shows the timing of various signals during power-up and power-down. The signals are:

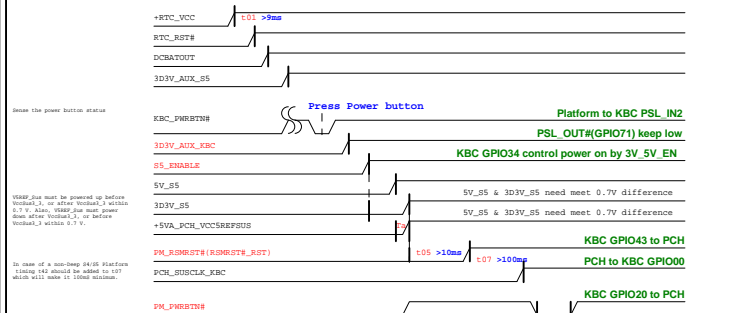
- 3DV_VGA_S0**: A signal that transitions from low to high during power-up and back to low during power-down.
- DGPIU_PWR_EN**: A signal that transitions from low to high during power-up and back to low during power-down.
- VGA_CORE**: A signal that transitions from low to high during power-up and back to low during power-down.
- DGPIU_PWBOK**: A signal that transitions from low to high during power-up and back to low during power-down.
- 1DSV_VGA_S0**: A signal that transitions from low to high during power-up and back to low during power-down.
- 1DSV_VGA_S0_PEX_VDD**: A signal that transitions from low to high during power-up and back to low during power-down.
- 1DSV_VGA_S0_PEX_VDD**: A signal that transitions from low to high during power-up and back to low during power-down.

Annotations include:

- PCH GPIO54 output**: Points to the 3DV_VGA_S0 signal.
- RT8208 PGOOD**: Points to the DGPIU_PWBOK signal.
- PEX_VDD**: Points to the 1DSV_VGA_S0_PEX_VDD signal.
- LPPOWER-OFF <10ms**: Points to the power-down sequence.

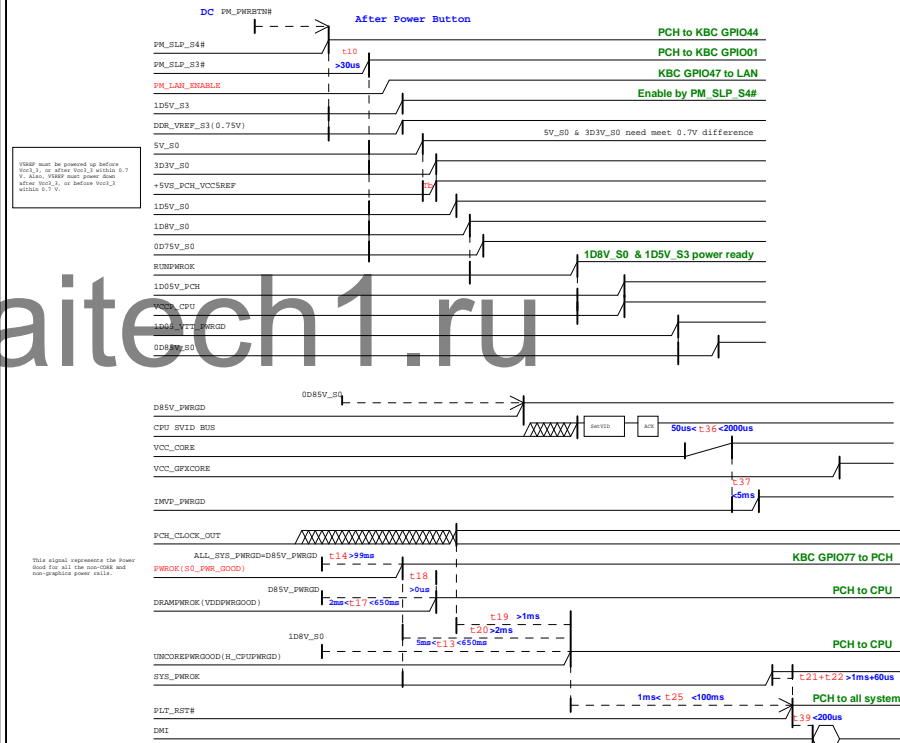
For power-down, reversing the ramp-up sequence is recommended.

Red Words: Controlled by EC GPIO



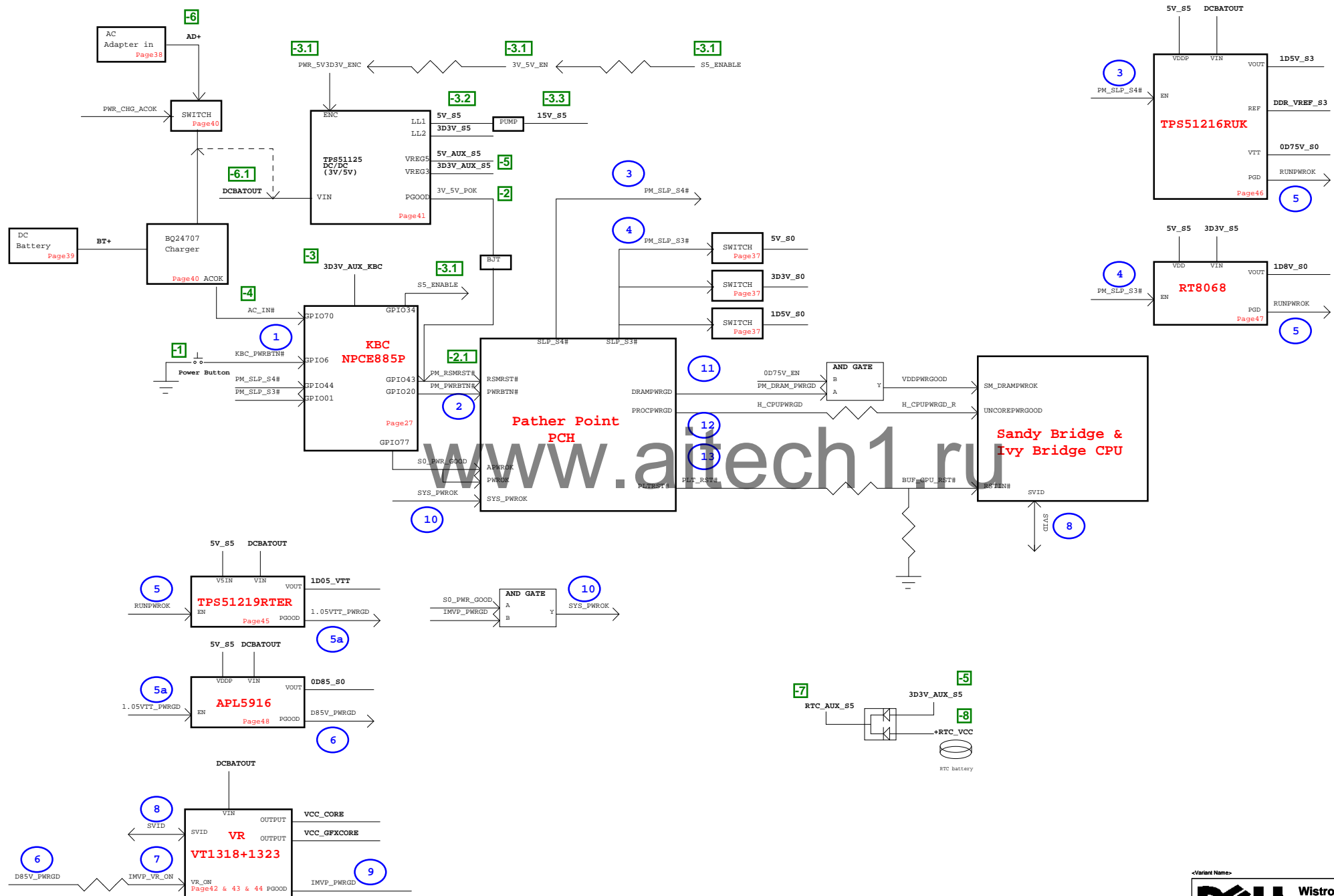
VREF_Sus must be powered up before VccSua1_3, or after VccSua1_3 within 0.7 V. Also, VREF_Sus must power down after VccSua1_3, or before VccSua1_3 within 0.7 V.

In case of a non-Deep 24/25 Platform
timing t42 should be added to t07
which will make it 100ns minimum.

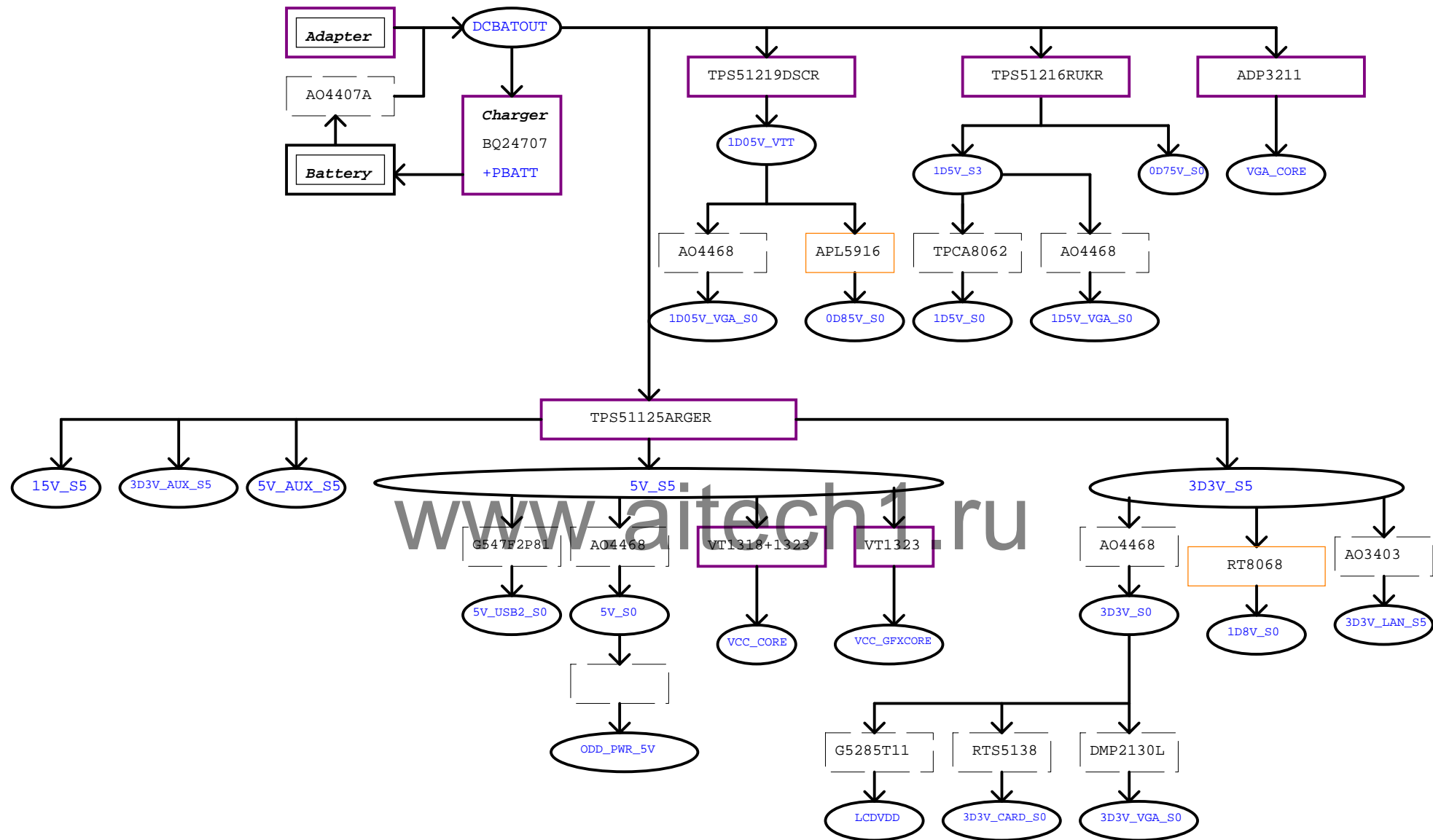


This signal represents the Power Good for all the non-CORE and non-graphics power rails.

DV14 MLK Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13



Power Shape

Regulator

LDO

Switch

<Variant Name>



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Title

Power Block Diagram

Size
A3

Document Number

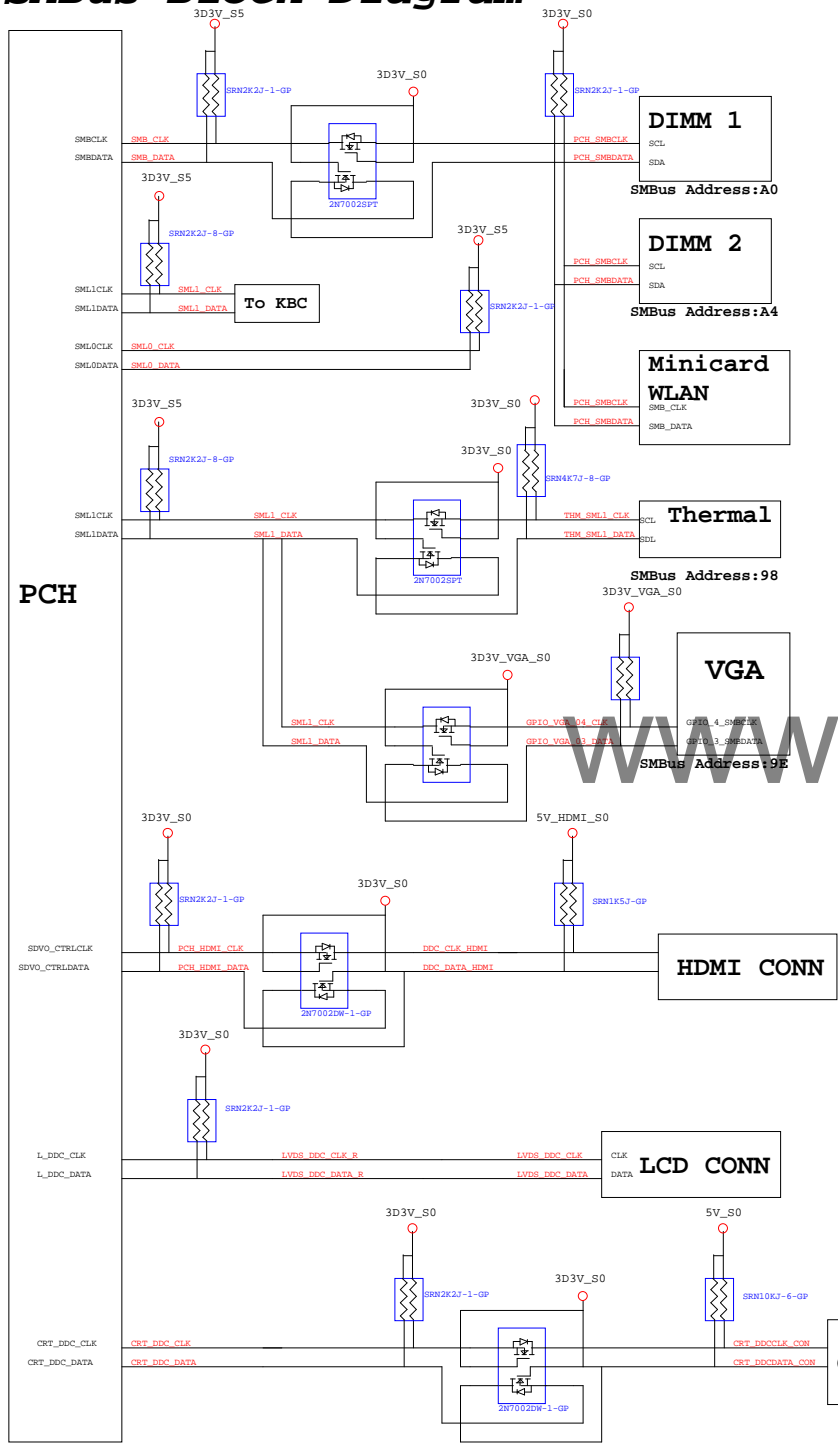
Enrico Caruso 14 MLK DIS

Rev
X02

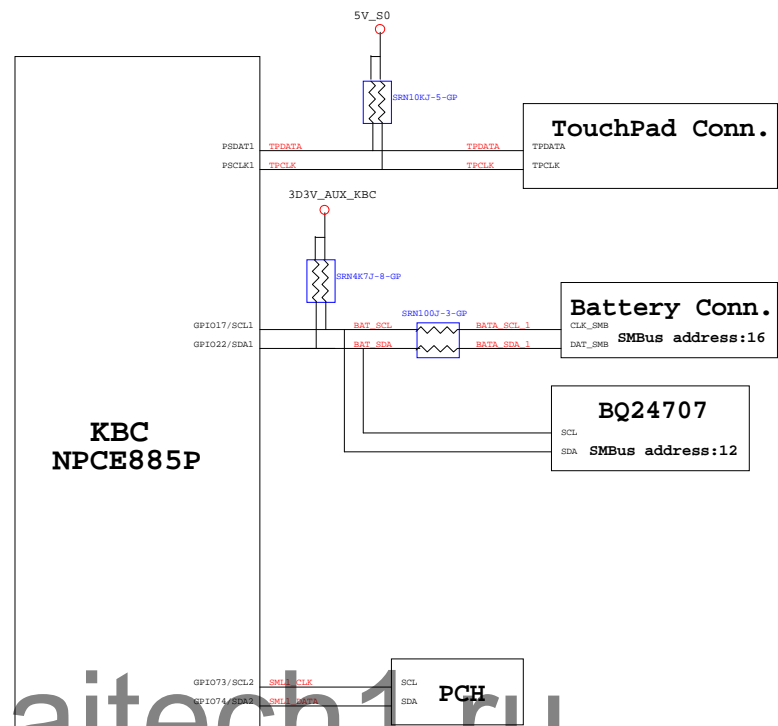
Date: Friday, December 30, 2011

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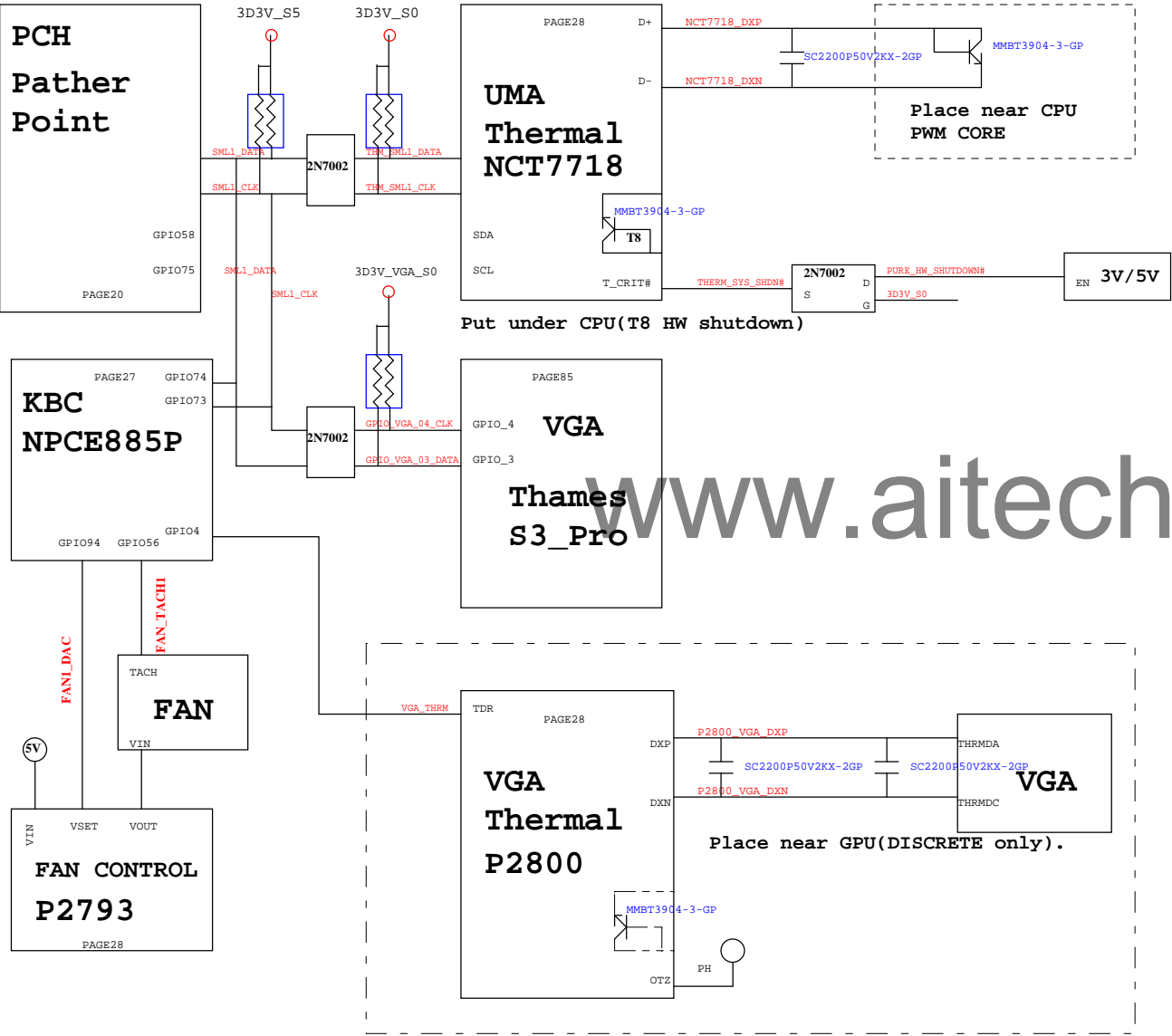
PCH SMBus Block Diagram



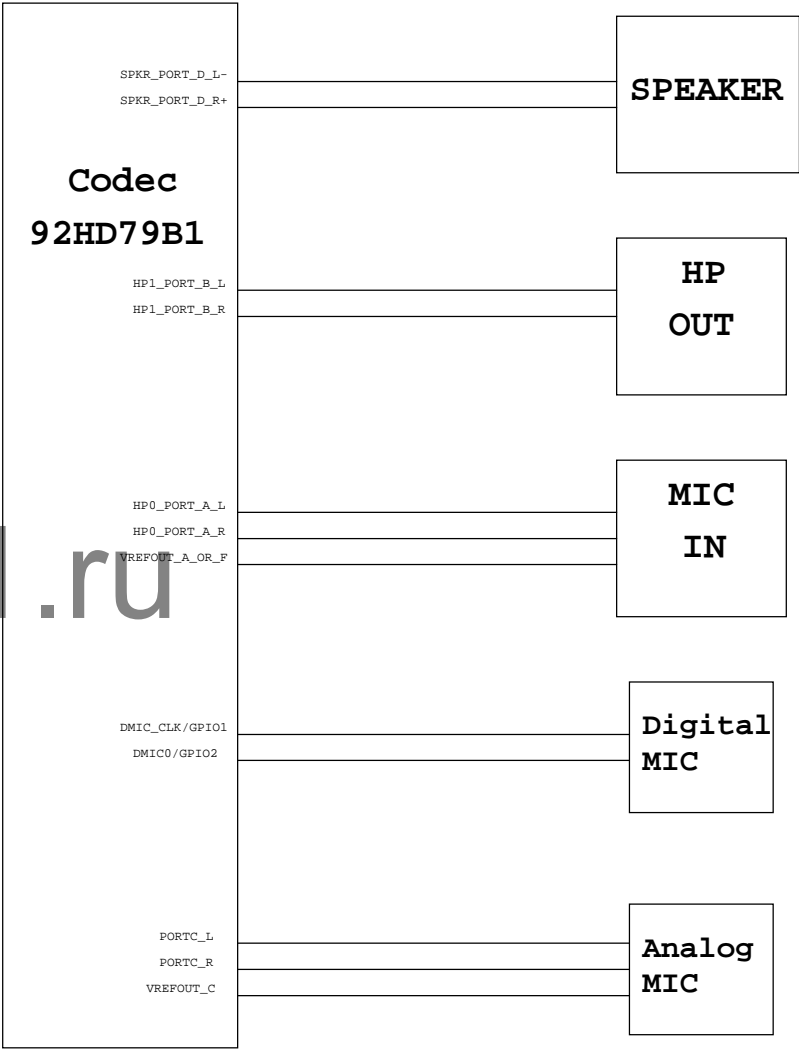
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



VERSION	DATA	PAGE	Change Item
X01	11/03	92	change PU9201 pin24 from 5V_S0 to 5V_S5 to avoid 5V_S0 leakage issue
	11/03	92	change PR9219 from 10K to 0ohm and DY PC9201 to adjust VGA_CORE sequence
	11/03	93	change PR9314 from 470 ohm to 220ohm to adjust 3D3V_VGA_S0 power down sequence
	11/08	40	change PC4010 from 78.47422.2QL to 78.47422.2BL to correct wistron Part number
	11/08	86	change VGA strap pin follow NV FAE suggest
	11/08	42	change PR4120 from 10K to 9.76K to adjust 5V_S5 from 5.0V to 5.07V
	11/09	36	change R3605 from 10K to 0 ohm,R3607 and R3630 from 10K to 100K, C3610 from 0.01 uF to 0.047 uF to adjust 3D3V_S0, 5V_S0 and 1D5V_S0 power sequence
	11/09	17	change RN1703 from 33 ohm to 22 ohm to solve CRT HSYNC and VSYNC rise and fail time issue
	11/09	50	change L5001 L5002 L5003 to 68.00084.931 to solve CRT RGB rise and fall time fail issue
	11/09	40 38 97	stuff EC4002,EC9709,EC9701,EC9705,EC9708,EC9702,EC9703,EC9704,EC9738,EC9710,EC4001,EC9707,EC9713,EC9715,EC9716,EC9720,EC9718,EC9712,EC9714,PC4120,EC9717,EC9719,EC9722,PC3801,EC9706,SPR1,SPR3,SPR4 for EMI request
	11/09	27	change R2724 from 10K to 20K for PCB version change
	11/09	86	change ROM_SLK_D4 to SMB_ALT_ADDR follow NV Design Guide
	11/09	86	change ROM_SO_C4 to VGA_DEVICE follow NV Design Guide
	11/09	86	change ROM_SI_D3 to SUB_VENDOR follow NV Design Guide
	11/09	86	change STRAP0_STRAP3 to RAM_CFG[0]_RAM_CFG[3] follow NV Design Guide
	11/09	86	change STRAP4 to PCIE_MAX_SPEED follow NV Design Guide
	11/10	22 83	dummy R8319 R8307 R2205 stuff U8301 and add R2202 to pull high DGPU_HOLD_RST# to 3D3V_S0 follow NV FAE suggest
	11/10	21	seperate RN2203 to R2205 and R2206 for bom control
	11/11	41	change PR4102 from 51K to 61.9K to set 5V OCP
	11/11	41	change PR4101 from 120K to 91K to set 3.3V OCP
	11/11	42	change PR4236 from 1.78K to 2.05K for CPU Loadline adjustment
	11/11	42	change PR4264 from 20K to 18.2K for CPU Loadline adjustment
	11/11	42	change PR4239 from 0 ohm to 191 ohm for GFX Loadline adjustment
	11/11	42	change PR4249 from 7.87K to 7.5K for GFX Loadline adjustment
	11/11	46	change PR4602 from 52.3K to 80.6K to Set 1.5V OCP
	11/11	92	change PR9238 from 133K to 196K and PR9225 from 3.83K to 2.26K for Loadline adjustment follow Nvidia SPEC
	11/11	45	dummy PR4506 and PR4507, Pop PR4505 and 3D3V_S0 change 3D3V_S5 for power team request
	11/11	29	install R2909,R2910,D2902 as to audio chip will change to 4213D
	11/14	92	change PC9213 PC9214 PC9216 to 78.10622.51L for power team request
	11/15	29	change R2909 R2910 to 0 ohm for vendor request
	11/15	61 82	stuff TR8201 TR8202 TR6101,dummy R6102 R6203 R8201 R8202 R8203 R8204 for EMI request
	11/16	39	add test point AFTP3902

VERSION	DATA	PAGE	Change Item
X01	11/16	31	change C3102 C3103 to 15pF for vendor suggest
	11/16	86	change C8610 C8611 to 10pF for vendor suggest
	11/23	88 89	change R8807 R8908 from 80.6 ohm to 162 ohm for NV FAE suggest
	11/24	83	change L8302 to 0 ohm for NV FAE suggest
X02	12/16	20	reserve R2005 10K Pull High for PEG-CLKREQ#_L
	12/16	29	change R2945 to 2.2K,accuracy 'J' follow vendor suggestion to solve internal mic too low issue
	12/22	88	DY C8815 C8816,stuff C8809 to avoid HDD interfere.
	12/23	22	DY R2202,stuff R2205 to pull low DGPU_HOLD_RST# to follow NV Design Guide
	12/23	20 83	DY R2004,stuff R2005 to pull high PEG_CLKREQ# to 3D3V_S5,stuff R8302 to pull high VGA_PEG_CLKREQ#,stuff Q8301 follow NV suggestion
	12/27	28	exchange the name of AFTP2801 and AFTP2802 to stay same with UMA for AFTP request
	12/28	40	add 0.1uF caps EC4004(BT+_R to GND) and EC4003(PWR_DCBATOUT_CHG to GND) to reduce EMI noise
	12/28	27	change R2724 from 20K to 33K for PCB version change
	12/29	88	remove C8815 to avoid HDD interfere follow NV suggestion
	12/29	32 51 65	changed R3206,R3207 to short pad,removed TR3201 CMC footprint;changed R5101,R5102,R5103, R5104,R5105,R5106,R5107,R5108 to short pad,removed TR5101,TR5102,TR5103,TR5104,CMC footprint;changed R6505,R6506 to short pad,removed TR6501 CMC footprint follow EMI suggestion
	12/29	51 41 15 18 19 23 24 27 28 29 31 32 36 37 44 46 51 65 68 83 86	change R504 R1404 R1405 R1503 R1504 R1807 R1906 R1910 R1912 R1913 R1924 R1929 R2306 R2307 R2308 R2402 R2403 R2404 R2720 R2723 R2761 R2764 R2765 R2766 R2767 R2768 R2778 R2792 R2794 R2807 R2813 R2905 R2906 R3105 R3208 R3605 R3614 R3708 R3710 R5101 R5102 R5103 R5104 R5105 R5106 R5107 R5108 R5125 R6505 R6506 R6510 R6511 R6804 R6805 R6811 R6813 R8503 R8607 / L8302 L8601 R2304 R2412 R3104 R3115 R3117 R3206 R3207 R4908 / R2301 R2911 R2912 / RN2010 RN2012 RN2014 RN2016 RN5002 / PR4212 PR4116 PR4121 PR4127 PR4252 PR4254 PR4251 PR4250 PR4261 PR4220 PR4232 PR4244 PR4304 PR4305 PR4403 PR4611 PR4607 from 0ohm to short pad
	12/29	58	change EC5801 EC5802 EC5803 EC5804 to 1000P cap for EMI request
	12/30	29	add 100K R2913 resistor in AUD_PC_BEEP let voltage can be discharged fast
	12/30	61 82	remove R6102,R6103;R8201,R8202;R8203,R8204 co-lay position;use CMC solution
	12/30	27	change R2735 from 10K to 20K to reduce inrush current of 3D3V_AUX_KBC
	12/30	41	change PC4126,PC4127 to 4.7u from 10u follow power team's suggestion
	12/30	27 86	remove TP2713,add R2713 for pull high OVER_CURRENT_P8# to 3D3V_AUX_KBC;add R8608,Q8603; change Q8603.2 to OVER_CURRENT_P8# from AC_PRESENT for OC trigger IPCC function
	12/30	58	stuff 1000pF EC5801 EC5802 EC580 EC5804 for EMI request
	01/03	49	remove R4903,R4904 co-lay position;use CMC solution
	01/03	45	change PR4510 to 82.5K from 69.8K to modify OCP follow power team's suggestion

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File

Change History

Size
A3

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Enrico Caruso 14 MLK DIS

Rev

X02

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